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COMMITTEE LETTER BALLOT

Committee: JC42.3

Committee Item Number: xxxx.yy

Subject: DDR5 Full Spec Draft Rev0.1

Background: All red and black items are for ballot, red text identifies the updates from the previous ballot. Items in grey are not part of the ballot material and are for reference only

Keywords: DDR5, Full Specification

PROPOSED

REVISION HISTORY

Revision	Author	Date	Status and Description
Rev0.1	C.Cox	12/5/17	Initial Format Rev0.1 - Includes all ballots through Q3'17

Document Formating Legend

Colors used in this Document and what they mean:

RED - All Red text is defined as something that is NEW

BLACK - Is considered the standard or the current Ballot.

LIGHT GREY - All Light Grey text is defined as something that should be considered TBD. The content may be accurate or the same as previous technologies but has not yet been reviewed or determined to be the working assumption.

Special NOTE: Some legacy diagrams that have not been updated may be BLACK or RED but that does not indicate that they are new or current working assumption. In the case where there is a digram that is BLACK or RED, it is important to look at the section for reference. If the section/heading is BLACK or RED, then it is as intended. If the section/heading is GREY, then assume its only an artifact of the old diagram that could not easily be changed.

1 Scope

This document defines the DDR5 SDRAM specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this Standard is to define the minimum set of requirements for JEDEC compliant 8Gb through 32Gb for x4, x8, and x16 DDR5 SDRAM devices. This standard was created based on the DDR4 standards (JESD79-4) and some aspects of the DDR, DDR2, DDR3 & LPDDR4 standards (JESD79, JESD79-2, JESD79-3 & JESD209-4).

2 DDR5 SDRAM Package, Pinout Description and Addressing

2.1 DDR5 SDRAM Row for X4, X8 - Q3’17 Ballot#1830.69B

The DDR5 SDRAM x4/x8 component will have 13 electrical rows of balls. Electrical is defined as rows that contain signal ball or power/ground balls. There may be additional rows of inactive balls for mechanical support.

2.2 DDR5 SDRAM Ball Pitch - Q3’17 Ballot#1830.69B

The DDR5 SDRAM component will use a ball pitch of 0.8mm by 0.8mm.
The number of depopulated columns is 3.

2.3 DDR5 SDRAM Columns for X4, X8 - Q3’17 Ballot#1830.69B

The DDR5 SDRAM x4/x8 component will have 6 electrical columns of balls in 2 sets of 3 columns.
There will be columns between the electrical columns where there are no balls populated.The number of these is 3.
Electrical is defined as columns that contain signal ball or power/ground balls. There may be additional columns of inactive balls for mechanical support.

2.4 DDR5 SDRAM X4/8 Ballout using MO-xxx - Q3'17 Ballot #1830.69B

	1	2	3	4	5	6	7	8	9	
A	RFU	VSS	VPP				ZQ	VSS	RFU	A
B	VDD	VDDQ	DQ2				DQ3	VDDQ	VDD	B
C	VSS	DQ0	DQS_t				DM_n, DBI_n, TDQS_t	DQ1	VSS	C
D	VDDQ	VSS	DQS_c				TDQS_c	VSS	VDDQ	D
E	VDD	DQ4	DQ6				DQ7	DQ5	VDD	E
F	VSS	VDDQ	VSS				VSS	VDDQ	VSS	F
G	CA_ODT	MIR	VDD				CK_t	VDDQ	TEN	G
H	ALERT_n	VSS	CS_n				CK_c	VSS	VDD	H
J	VDDQ	A4	A0				A1	A5	VDDQ	J
K	VDD	A6	A2				A3	A7	VDD	K
L	VDDQ	VSS	A8				A9	VSS	VDDQ	L
M	CAI	A10	A12				A13	A11	RESET_n	M
N	VDD	VSS	VDD				VPP	VSS	VDD	N

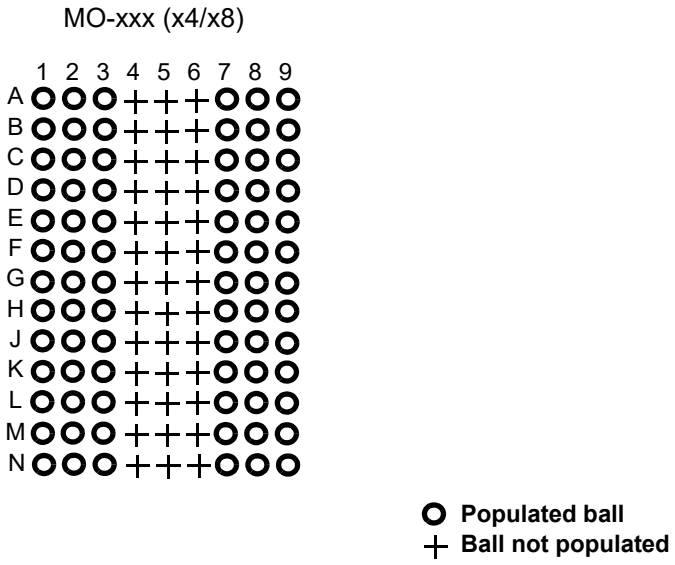
Notes:

* DQ4-DQ7 are higher order DQ pins and are not connected for the x4 configuration.

** TDQS_t is not valid for the x4 configuration.

*** TDQS_c is not available for the x4 configuration.

Figure 1 — DDR5 Ball Assignments for the x4/8 component



2.5 DDR5 SDRAM X16 Ballout using MO-xxx - No Ballot

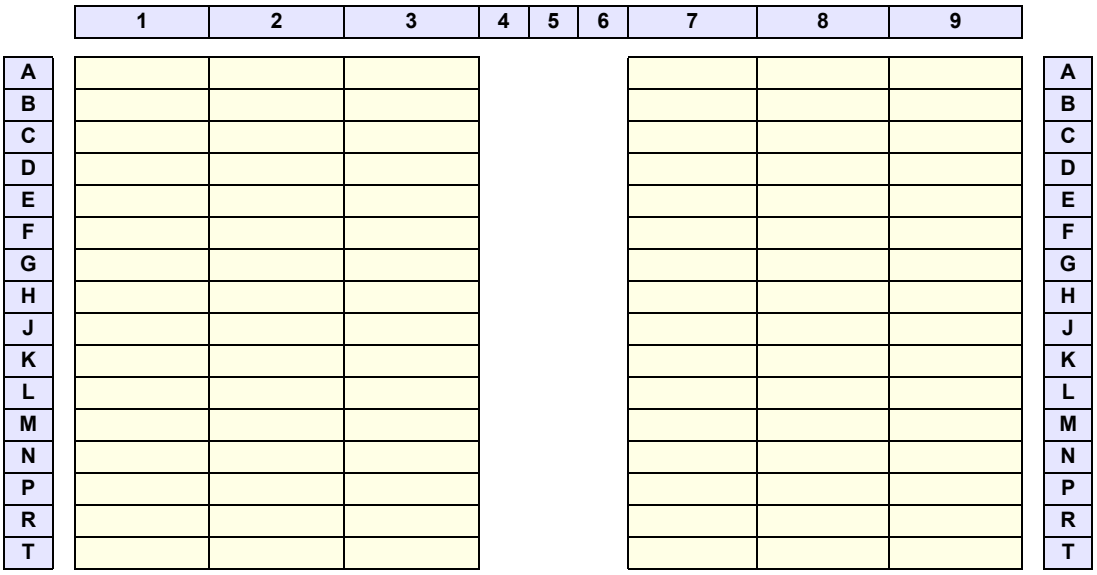
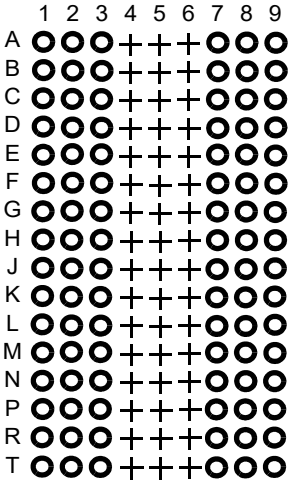


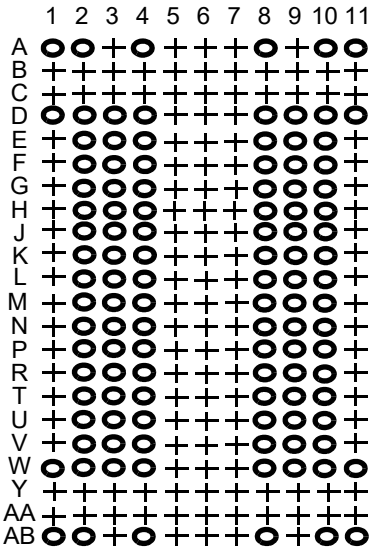
Figure 2 — DDR5 Ball Assignments for the x16 component

MO - xxx Variation DU-z (x16)



Populated ball
Ball not populated

MO-xxx Variation DY-z (x16)
with support balls



2.6 Pinout Description - Q4'16 Ballot #1830.69

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CS_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code. CS is also used to enter and exit the parts from power down modes.
DM_n/DBI_n/ TDQS_t, (DMU_n/ DBIU_n), (DML_n/ DBIL_n)	Input/Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR5 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in X8
CA [13:0]	Input	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi-cycle, the pins may not be interchanged between devices on the same bus.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DD},
DQ	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting TBD. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific data sheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DBI/TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11,12,10and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
ALERT_n	Input/Output	Alert : It has multi functions such as CRC error flag , Command and Address Parity error flag as Output signal. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.
TEN	Input	Connectivity Test Mode Enable: Required on X4,X8 & X16 devices. HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
MIR	Input	Mirror: Used to inform the system that this device is being run in Mirrored mode vs. Standard mode. Support for this device removes the need for a custom mirrored package. With the MIR pin connected to VDDQ, the SDRAM internally swaps even numbered CA with the next higher odd number CA. Normally the MIR pin must be tied to VSSQ if no CA mirror is required. Mirror pair examples: CA2 with CA3 (not CA1) CA4 with CA5 (not CA3).
CAI	Input	Command & Address Inversion: With the CAI pin connected to VDDQ, DRAM internally inverts the logic level present on all the CA signals. Normally the CAI pin must be connected to VSSQ if no CA inversion is required.
CA_ODT	Input	ODT for Command and address enabled, if the pin is connected to VDD and disabled, if the pin is connected to VSS
RFU	Input/Output	Reserved for future use

Symbol	Type	Function
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.1 V +/- 0.055 V
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.1 V +/- 0.055 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 1.8V Nom, 1.71V Min, 1.98V Max
ZQ	Supply	Reference Pin for ZQ calibration
NOTES:		

2.7 DDR5 SDRAM Addressing - Q2'17 Item#1830.36B

8 Gb Addressing Table

Configuration		2 Gb x4	1 Gb x8	512 Mb x16
Bank Address	# of Bank Groups	8	8	4
	BG Address	BG0~BG2	BG0~BG2	BG0~BG1
	Bank Address in a BG	BA0	BA0	BA0
Row Address		R0~R15	R0~R15	R0~R15
Column Address		C0~C10	C0~C9	C0~C9
Page size		1KB	1KB	2KB

16 Gb Addressing Table

Configuration		4 Gb x4	2 Gb x8	1 Gb x16
Bank Address	# of Bank Groups	8	8	4
	BG Address	BG0~BG2	BG0~BG2	BG0~BG1
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
Row Address		R0~R15	R0~R15	R0~R15
Column Address		C0~C10	C0~C9	C0~C9
Page size		1KB	1KB	2KB

24 Gb Addressing Table

Configuration		6 Gb x4	3 Gb x8	1.5 Gb x16
Bank Address	# of Bank Groups	8	8	4
	BG Address	BG0~BG2	BG0~BG2	BG0~BG1
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
Row Address[1]		R0~R16	R0~ R16	R0~R16
Column Address		C0~C10	C0~C9	C0~C9
Page size		1KB	1KB	2KB

Note 1 Row address R[16:15] of 00b, 01b, and 10b are valid. Row address R[16:15] of 11b is invalid.

32 Gb Addressing Table

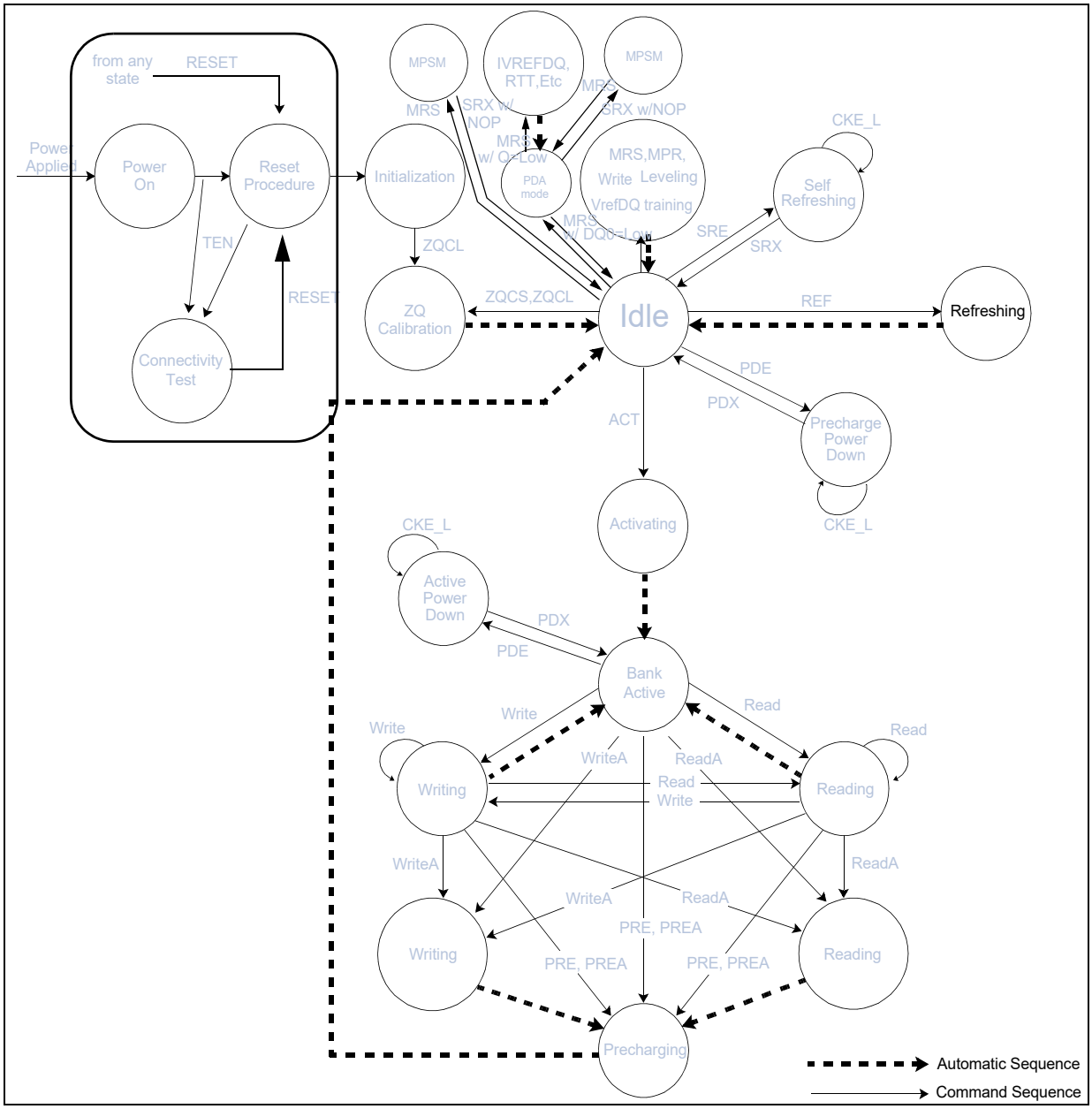
Configuration		8 Gb x4	4 Gb x8	2 Gb x16
Bank Address	# of Bank Groups	8	8	4
	BG Address	BG0~BG2	BG0~BG2	BG0~BG1
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
Row Address		R0~R16	R0~R16	R0~R16
Column Address		C0~C10	C0~C9	C0~C9
Page size		1KB	1KB	2KB

64 Gb Addressing Table

Configuration		16 Gb x4	8 Gb x8	4 Gb x16
Bank Address	# of Bank Groups	8	8	4
	BG Address	BG0~BG2	BG0~BG2	BG0~BG1
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
Row Address		R0~R17	R0~R17	R0~R17
Column Address		C0~C10	C0~C9	C0~C9
Page size		1KB	1KB	2KB

3 Functional Description

3.1 Simplified State Diagram - No Ballot



Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Activate	Read	RD,RDS4, RDS8	PDE	Enter Power-down
PRE	Precharge	Read A	RDA, RDAS4, RDAS8	PDX	Exit Power-down
PREA	PRECHARGE All	Write	WR, WRS4, WRS8 with/without CRC	SRE	Self-Refresh entry
MRS	Mode Register Set	Write A	WRA,WRAS4, WRAS8 with/without CRC	SRX	Self-Refresh exit
REF	Refresh, Fine granularity Refresh	RESET_n	Start RESET procedure	MPR	Multi Purpose Register
TEN	Boundary Scan Mode Enable				

NOTE: 1. This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than on bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.

3.2 Basic Functionality - No Ballot

The DDR5 SDRAM is a high-speed dynamic random-access memory. To ease transition from DDR4 to DDR5, the introductory density (8Gb) will be internally configured as 16-banks, 8 bank group with 2 banks for each bank group for x4/x8 and 8-banks, 4 bank group with 2 banks for each bankgroup for x16 DRAM. When the industry transitions to higher densities (=>16Gb), it double the bank resources and internally be configured as 32-banks, 8 bank group with 4 banks for each bank group for x4/x8 and 16-banks, 4 bank group with 4 banks for each bankgroup for x16 DRAM.

The DDR5 SDRAM uses a 16n prefetch architecture to achieve high-speed operation. The 16n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR5 SDRAM consists of a single 16n-bit wide, eight clock data transfer at the internal DRAM core and sixteen corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR5 SDRAM are burst oriented, start at a selected location, and continue for a burst length of sixteen or a ‘chopped’ burst of eight in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command. The address bits registered with the ACTIVATE Command are used to select the bank and row to be activated (i.e. in a 16Gb part, BG0-BG2 in a x4/8 and BG0-BG1 in x16 select the bankgroup; BA0-BA1 select the bank; R0-R17 select the row; refer to “DDR5 SDRAM Addressing” for specific requirements). The address bits registered with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (TBD), and select BC8 or BL16 mode (TBD) if enabled in the mode register.

Prior to normal operation, the DDR5 SDRAM must be powered up and initialized in a predefined manner.

The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

3.3 RESET and Initialization Procedure - Q1'17 Ballot

For power-up and reset initialization, in order to prevent DRAM from functioning improperly default values for the following MR settings need to be defined.

Table 1 — MR default settings

Item	Mode Register	Default Setting	Description
Write Latency	MRxx OP[TBD]	TBD	WL = TBD
Read Latency	MRxx OP[TBD]	TBD	RL = TBD, RTP = TBD
Write Recovery	MRxx OP[TBD]	TBD	WR = TBD
DBI-WR/RD	MRxx OP[TBD]	TBD	Write and Read DBI are disabled
CA ODT	MRxx OP[TBD]	TBD	CA ODT is enabled/disabled based on strap value
DQ ODT	MRxx OP[TBD]	TBD	DQ ODT is defaulted to RTT_PARK
VREF(CA) Value	MRxx OP[TBD]	TBD	VREF(CA) Range: xx% of VDD
VREF(DQ) Value	MRxx OP[TBD]	TBD	VREF(DQ) Range: xx% of VDD
Per DRAM Addressability	MRxx OP[TBD]	TBD	PDA Disabled
Post Package Repair	MRxx OP[TBD]	TBD	PPR Disabled
Target Row Refresh	MRxx OP[TBD]	TBD	
TBD			

3.3.1 Power-up Initialization Sequence

The following sequence shall be used to power up the DDR5 device. Unless specified otherwise, these steps are mandatory.

1. While applying power (after Ta), RESET_n is recommended to be LOW (≤0.2 x VDD2) and all other inputs may be undefined. The device outputs remain disabled while RESET_n is held LOW. Power supply voltage ramp requirements are provided in Table 2. VPP must ramp at the same time or earlier than VDD.

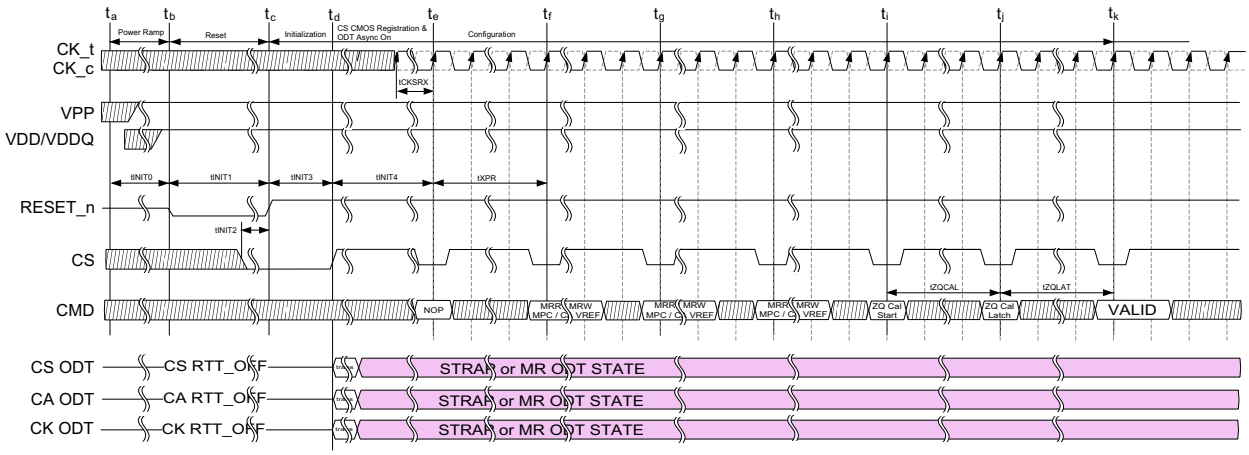
Table 2 — Voltage Ramp Conditions

After	Application Conditions
Ta is reached	VPP must be greater than VDD - x mV

Note:
1) Ta is the point when any power supply first reaches 300mV
2) Voltage ramp conditions in the table above apply between tA and Power-off (controlled or uncontrolled).
3) Tb is the point at which all supply and reference voltages are within their defined ranges.
4) Power ramp duration tINIT0 (Tb-Ta) must not exceed 200ms

2. Following the completion of the voltage ramp (Tb), RESET_n must be maintained LOW. DQ, DQS_t, DQS_c, voltage levels must be between VSSQ and VDDQ to avoid latch-up. CS_n, CK_t, CK_c and CA input levels must be between VSS and VDD to avoid latch-up.

3. Beginning at Tb, RESET_n must be maintained LOW for a minimum of tINIT1 (Tb to Tc), after which RESET_n can be deasserted to HIGH (Tc). At least tINIT2 (10ns) before RESET_n de-assertion, CS is required to be set LOW. All other input signals are "Don't Care". The DRAM needs to support the ability for RESET_n to be held indefinitely.



NOTE 1 From time point 'Td' until 'Tk', DES commands must be applied between legal commands (MRR/MRW/MPC & VREFCA).
NOTE 2 MR Commands must be issued to all Mode Registers that have defined settings.

Figure 3 — RESET_n and Initialization Sequence at Power-on Ramping

4. After RESET_n is de-asserted (Tc), wait at least tINIT3 (2ms) before driving CS high.

5. After setting CS high (Td), wait a minimum of tINIT4 to allow the DRAM CMOS based receiver to register the exit and allow the CS, CK & CA ODT to go to the defined strap or MRS state (Te). Upon the completion of Te, CA, CS and CK ODT states should be valid and the DRAM's CS receiver should no longer be in it's CMOS based mode. Clock (CK_t,CK_c) is required to be started and stabilized for tCKSRX before exit of tINIT4 (Te).

6. Upon Te, a NOP must be issued to conclude exit of initialization process and start tXPR timer. The system must wait at least tXPR before issuing any legal configuration commands (Tf). During configuration, only MRR, MRW, MPC and VREFCA commands are legal.

7. Between Tf to Ti, any number of legal configuration commands are allowed. Training based commands are optional and may be done at the system architects discretion and may vary depending on the systems.

8. Upon completing all configuration commands (Ti), the DRAM controller can issue a ZQ Cal Start command to the memory. This command is used to calibrate VOH level and output impedance over process, voltage and temperature. ZQ calibration sequence is completed after tZQCAL (Tj) and the ZQ Cal Latch command must be issued to update the DQ drivers and the DQ+CA ODT to calibrated values.

9. After tZQLAT is satisfied (Tk), the DDR5 device is ready for normal operation and is able to accept any valid command. Any ore register that have not previously been set up for normal operation should be written at this time.

Table 3 — Initialization Timing Parameters

Parameter	Value		Unit	Comment
	Min	Max		
tINIT0	-	200	mS	Maximum voltage-ramp time
tINIT1	200		uS	Minimum RESET_n LOW time after completion of voltage ramp
tINIT2	10	-	nS	Minimum CS LOW time before RESET_n HIGH
tINIT3	2	-	mS	Minimum CS LOW time after RESET_n HIGH
tINIT4	TBD	-	nS	Minimum time for DRAM to register EXIT on CS with CMOS.
tXPR	TBD	-	nS	Minimum time from Exit Reset to first valid Configuration Command
tCKSRX	SEE Self Refresh Timing Table			Minimum stable clock time

3.3.2 TBD - VDD Slew rate at Power-up Initialization Sequence

Table 4 — VDD Slew Rate

Symbol	Min	Max	Units
VDD_sl[a]	0.004	600	V/ms[b]
VDD_ona		200	ms[c]

a.Measurement made between 300mv and 80% Vdd minimum.
b.20 MHz bandlimited measurement.
c.Maximum time to ramp VDD from 300 mv to VDD minimum.

3.3.3 TBD - Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization as shown in Figure 5.

FIGURE TBD

NOTE 1 From time point 'Td' until 'Tk', DES commands must be applied between MRS and ZQCL commands
NOTE 2 MRS Commands must be issued to all Mode Registers that have defined settings.

Figure 4 — Reset Procedure at Power Stable

3.4 Mode Register Definition - Q1'17 Ballot #1845.17

3.4.1 Mode Register Read (MRR)

The Mode Register Read (MRR) command is used to read configuration and status data from the DDR5-SDRAM registers. The MRR command is initiated with CS and CA[13:0] in the proper state as defined by the Command Truth Table. The mode register address operands (MA[7:0]) allow the user to select one of 256 registers. The mode register contents are available on the second 8 UI's of the burst and are repeated across all DQ's after the RL following the MRR command. To avoid a potentially worst cast pattern, every odd DQ bit (represented with !) will have its contents inverted. Data in the burst (BL0-7) will be either "0" or "1", with "1" indicating that the content of the later UI's (BL8-15) are inverted. DQS is toggled for the duration of the Mode Register READ burst. The MRR has a command burst length 16.
MRR operation must not be interrupted. Non-Target ODT encoding is available for MRR just like a normal READ.

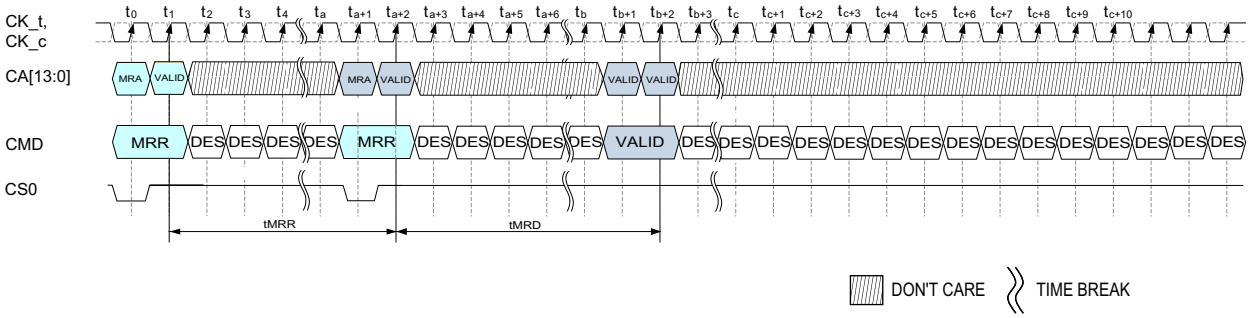


Figure 5 — Mode Register Read Timing

Table 5 — DQ output mapping

BL	0-7	8	9	10	11	12	13	14	15
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ4	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ5	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ6	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ7	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ8	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ9	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ10	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ11	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ12	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ13	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ14	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ15	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7

Notes:
1. DBI may or may not apply during normal MRR. It's vendor specific. If read DBI is enable with MRS and vendor cannot support the DBI during MRR, DMI pin status should be low
2. The read pre-amble and post-amble of MRR are same as normal read.
3. The number of DQ's vary based on the IO width of the device. x4 supports only DQ0-3, while x8 supports DQ0-7 and x16 supports DQ0-15.

3.4.2 Mode Register WRITE (MRW)

The Mode Register Write (MRW) command is used to write configuration data to the mode registers. The MRW command is initiated with CS and CA[13:0] in the proper state as defined by the Command Truth Table. The mode register address and the data written to the mode registers is contained in CA[13:0] according to the Command Truth Table. The MRW command period is defined by tMRW. Mode register Writes to read-only registers have no impact on the functionality of the device.

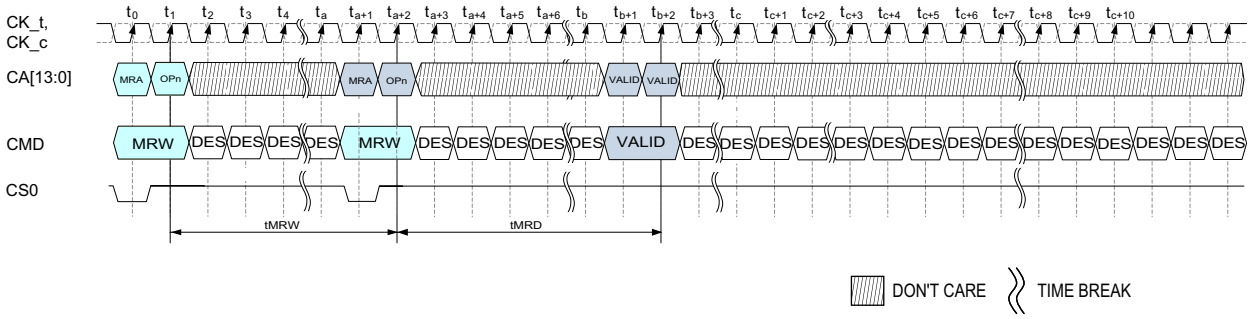


Figure 6 — Mode Register Write Timing

3.4.3 Mode Register Truth Tables and Timing Constraints

Table 6 — Mode Register Read/Write AC timing

Parameter	Symbol	Min/ Max	Value	Unit	Note
Mode Register Read/Write Timing					
Additional time after tXP has expired until MRR command may be issued	tMRRI	Min	tRCD + 3nCK	-	
Mode Register Read command period	tMRR	Min	16	nCK	
Mode Register Read Pattern to Mode Register Read Pattern Command spacing	tMRR_p	Min	8	nCK	
Mode Register Write command period	tMRW	Min	MAX(10ns, 16nCK)	-	
Mode Register Set command delay	tMRD	Min	max(14ns, 16nCK)	-	

Table 7 — Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW)

Current State	Command	Intermediate State	Next State
SDRAM		SDRAM	SDRAM
All Banks Idle	MRR	Mode Register Reading (All Banks Idle)	All Banks Idle
	MRW	Mode Register Writing (All Banks Idle)	All Banks Idle
Bank(s) Active	MRR	Mode Register Reading	Bank(s) Active
	MRW	Mode Register Writing	Bank(s) Active

Table 8 — MRR/MRW Timing Constraints: DQ ODT is Disable

From Command	To Command	Minimum Delay between "From Command" and "To Command"	Unit	Notes
MRR	MRR	tMRR	-	
	RD	tMRR	-	
	WR MRW	RL+RU(tDQSCK(max)/tCK)+BL/2+ 3 -WL	nCK	
	MRW	RL+RU(tDQSCK(max)/tCK)+BL/2+ 3	nCK	
RD	MRR	BL/2	nCK	
WR/MRW		WL+1+BL/2+RU(tWTR/tCK)	nCK	
MRW		tMRD	-	
Power Down Exit		tXP+tMRRI	-	
MRW	RD	tMRD	-	
	WR/ MRW	tMRD	-	
	MRW	tMRW	-	
RD	MRW	RL+BL/2+RU(tDQSCKmax/tCK) +RD(tRPST) +max(RU(7.5ns/tCK),8nCK)	nCK	
WR/MRW		WL+1+BL/2+max(RU(7.5ns/tCK),8nCK)	nCK	

Table 9 — MRR/MRW Timing Constraints: DQ ODT is Enable

From Command	To Command	Minimum Delay between "From Command" and "To Command"	Unit	Notes
MRR	MRR	Same as ODT Disable Case	-	
	RD			
	WR/ MRW	RL+RU(tDQSCK(max)/tCK)+BL/2+3 -ODTLon-RD(tODTon(min)/tCK)	nCK	
	MRW	Same as ODT Disable Case	-	
RD	MRR	Same as ODT Disable Case	-	
WR/ MRW				
MRW				
Power Down Exit				
MRW	RD	Same as ODT Disable Case	-	
	WR/ MRW			
	MRW			
RD	MRW	Same as ODT Disable Case	nCK	
WR/ MRW/ WR FIFO				

3.5 Mode Registers - Q1'17 Ballot #1845.17 (OUT OF DATE)

With DDR5, the utilization and programming method will change from the traditional addressing scheme found in DDR3 and DDR4, and will move to the method used by LPDDR, where the Mode Register Addresses (MRA) and Payload placed in Op Codes (OP) are all packeted in the command bus encoding method. Please refer to the Command Truth Table 11 for Mode Register Read (MRR) and Mode Register Write (MRW) command protocol.

For DDR5, the SDRAM will support up to 8 MRA's, each with a byte wide payload. Allowing for up to 256 byte wide registers.
NOTE: Initial designs may not utilize all of this space, and for simplicity, only the first 64 will be shown.

3.5.1 Mode Register Assignment and Definition in DDR5 SDRAM

Table 10 shows the mode registers for DDR5 SDRAM. Each register is denoted as "R" if it can be read but not written, "W" if it can be written but not read, and "R/W" if it can be read and written. A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register

Table 10 — Mode Register Assignment in DDR5 SDRAM

MR#	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
0	CL						BL	
1	RFU	CWL					RFU	
2	RFU					Write Level-ing Init	Write Leveling	Read Preamble Training
3	DLL Reset	DLL Delay Frozen	DLL Enable	RFU	RFU	RFU	PDA Mode	2N Mode
4	RFU		Refresh tRFC Mode		Refresh Rate			Temp Sensor
5	Rd DBI Enable	Wr DBI Enable	DM Enable	TBD	Int VREF Mon	ODI		Data Output Disable
6	RFU				Write Recovery / RTP			
7	RFU	CRC WR Latency			CRC Write Err Status	RFU	Read CRC	Write CRC
8	RFU				Write Preamble Setting		Read Preamble Setting	
9	VrefCA Cal enable	VrefDQ Cal enable	RFU					
10	VrefDQ Cal Settings							
11	VrefCA Cal Settings							
12	RFU				Data Rate			
13	RFU	tRP						RFU
14	Transparency Configuration							
15	Transparency Threshold Filter							
16	Reserved for Transparency							
17	Reserved for Transparency							
18	Reserved for Transparency							
19	Reserved for Transparency							
20	Reserved for Transparency							
21	Reserved for Transparency							
22	Reserved for Transparency							
23	RFU						sPPR	hPPR
24	RFU							
25	RFU							MPC Read Format
26	Read Training Data UI (7:0)							
27	Read Training Data UI (15:8)							
28	MPC Read Invert DQ7	MPC Read Invert DQ6	MPC Read Invert DQ5	MPC Read Invert DQ4	MPC Read Invert DQ3	MPC Read Invert DQ2	MPC Read Invert DQ1	MPC Read Invert DQ0
29	MPC Read Invert DQ15	MPC Read Invert DQ14	MPC Read Invert DQ13	MPC Read Invert DQ12	MPC Read Invert DQ11	MPC Read Invert DQ10	MPC Read Invert DQ9	MPC Read Invert DQ8
30	LFSR Assignment - Read Training Data							
31	NOT A REGISTER BUT ADDRESS RESERVED FOR READ TRAINING PATTERN							
32	RFU	RFU	CK ODT					

Table 10 — Mode Register Assignment in DDR5 SDRAM

33	RFU	RFU	CS ODT			CA ODT		
34	RFU	Unmatched DQS	RTT_WR			RTT_PARK		
35	ODT during PD	RFU	RTT_NOM_RD			RTT_NOM_WR		
36	RFU	RFU	ODTLoff_WR			ODTLon_WR		
37	RFU	RFU	ODTLoff_WR_NT			ODTLon_WR_NT		
38	RFU	RFU	ODTLoff_RD			ODTLon_RD		
39	RFU	RFU	ODTLoff_RD_NT			ODTLon_RD_NT		
40	RFU	RFU	ODTLoff_DQS_WR			ODTLon_DQS_WR		
41	RFU	RFU	ODTLoff_DQS_WR_NT			ODTLon_DQS_WR_NT		
42	RFU	RFU	ODTLoff_DQS_RD			ODTLon_DQS_RD		
43	RFU	RFU	ODTLoff_DQS_RD_NT			ODTLon_DQS_RD_NT		
44	RFU					DQS Offset Timing		
45	DQS Interval Osc							
46	DQS Interval Osc							
47	DQS Interval Osc							
48	Write Pattern Mode							
49							Fast Zero Status	Fast Zero Mode
50								
51								
52								
53								
54								
55								
56								
57								
58								
59								
60								
61								
62								
63	DRAM Scratch Pad							

3.5.2 MR0 (MA[7:0]=00_H) - Q3'17 Ballot #1845.35B

MR0 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	CAS Latency					Burst Length	

Function	Register Type	Operand	Data	Notes
Burst Length	R/W	OP[1:0]	00_B: BL16 01_B: BC8 OTF 10_B: BL32 (Optional) 11_B: BL32 OTF (Optional)	
CAS Latency	R/W	OP[6:2]	00000_B: 18 00001_B: 19 ... 11110_B: 56 11111_B: RFU	
RFU		OP[7]	RFU	

Note - 1. PDA is entered & exited by the MPC command.

3.5.3 MR1 (MA [7:0] = 01_H) - PDA Mode Details - Q3'17 Ballot #1845.35B

MR1 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
PDA Select ID				PDA Enumerate ID			

Function	Register Type	Operand	Data	Notes
PDA Enumerate ID	R	OP[3:0]	This is a **Read Only** MR field, which is only programmed through an MPC command with the PDA Enumerate ID opcode. $xxxx_B$ Encoding is set with MPC command with the PDA Enumerate ID opcode. This can only be set when PDA Enumerate Programming Mode is enabled and the associated DRAM's DQ0 is asserted LOW. The PDA Enumerate ID opcode includes 4 bits for this encoding. Default setting is 1111_B	
PDA Select ID	R	OP[7:4]	This is a **Read Only** MR field, which is only programmed through an MPC command with the PDA Select ID opcode. $xxxx_B$ Encoding is set with MPC command with the PDA Select ID opcode. The PDA Select ID opcode includes 4 bits for this encoding. 1111_B = all DRAM's execute MRW, MPC, and VrefCA commands For all other encodings, DRAM's execute MRW, MPC, and VrefCA commands only if PDA Select ID[3:0] = PDA Enumerate ID[3:0], with some exceptions for specific MPC commands that execute regardless of PDA Select ID. Default setting is 1111_B	

NOTES:

3.5.4 MR2 (MA [7:0] = 02_H) - DQS Training - Q3'17 Ballot #1845.35B

MR2 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU					Write Leveling Init	Write Leveling	Read Preamble Enable

Function	Register Type	Operand	Data	Notes
Read Preamble Enable	R/W	**OP[0]**	**0_B: Normal Mode (Default)** **1_B: Read Preamble Training**	
Write Leveling	R/W	**OP[1]**	**0_B: Normal Mode (Default)** **1_B: Write Leveling**	
Write Leveling Init	R/W	**OP[2]**	**0_B: Disable (Default)** **1_B: Enable**	
RFU	TBD	**OP[7:3]**		

3.5.5 MR3 (MA[7:0]=03_H) - Functional Modes - Q3'17 Ballot #1845.33B

MR3 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DLL Reset	DLL Enable	RFU			CS Assertion Duration (MPC)	Max Power Savings Mode	2N Mode

Function	Register Type	Operand	Data	Notes
2N Mode	R	OP[0]	0_B: 2N Mode (Default) 1_B: 1N Mode	1
Max Power Savings Mode	R/W	OP[1]	0_B: Disable (Default) 1_B: Enable	
CS Assertion Duration (MPC)	R/W	OP[2]	0_B: Multiple cycles of CS assertion supported for MPC and VrefCA commands 1_B: Only a single cycle of CS assertion supported for MPC and VrefCA commands	
RFU		OP[5:3]	RFU	
DLL Enable	R/W	OP[6]	0_B: Disable 1_B: Enable (Default)	
DLL Reset	W	OP[7]	0_B: Normal (Default) 1_B: DLL Reset	

Note(s):
1 - This mode register is programmed via an explicit MPC command only.

3.5.6 MR4 (MA[7:0]=04_H) - Refresh Settings - Q1'17 Ballot #1845.32B w/Editorial update

MR4 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU			Refresh tRFC Mode	Refresh Rate			Temp Sensor

Function	Register Type	Operand	Data	Notes
Temp Sensor	R/W	OP[0]	0_B: Disable 1_B: Enable	
Refresh Rate	R	OP[3:1]	000_B: <Low Temp Range 001_B: 4x Ref Rate 010_B: 2x Ref Rate 011_B: Ref Rate (Default) 100_B: 0.5x Ref Rate 101_B: 0.25x Ref Rate 110_B: 0.125x Ref Rate 111_B: Exceeds High Temp Range	
Refresh tRFC Mode	R/W	OP[4]	0_B: Normal Refresh Mode (tRFC1) 1_B: Fine Granularity Refresh Mode (tRFC2)	
RFU	R/W	OP[7:5]	RFU	

3.5.7 MR5 (MA[7:0]=05_H) - IO Settings - Q2'17 Ballot #1845.31A

MR5 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Rd DBI Enable	Wr DBI Enable	DM Enable	TDQS Enable	RFU	Output Driver Impedance		Data Output Disable

Function	Register Type	Operand	Data	Notes
Data Output Disable	R/W	OP[0]	0_B: Normal Operation (Default) 1_B: Outputs Disabled	
Output Driver Impedance	R/W	OP[2:1]	00_B: RZQ/7 (34) 01_B: RFU 10_B: RZQ/5 (48) 11_B: RFU	
RFU	R/W	OP[3]	RFU	
TDQS Enable	R/W	OP[4]	0_B: Disable (Default) 1_B: Enable	
DM Enable	R/W	OP[5]	0_B: Disable (Default) 1_B: Enable	
Wr DBI Enable	R/W	OP[6]	0_B: Disable 1_B: Enable	
Rd DBI Enable	R/W	OP[6]	0_B: Disable 1_B: Enable	

NOTE:

3.5.8 MR6 (MA[7:0]=06_H) - Write Recovery Time & tRTP - Q2'17 Ballot #1845.31A

MR6 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
tRTP				Write Recovery Time			

Function	Register Type	Operand	Data	Notes
Write Recovery Time	R/W	OP[3:0]	0000_B: TBD nCK 0001_B: TBD nCK ... 1110_B: TBD nCK 1111_B: RFU (currently 45ns)	1
tRTP	R/W	OP[7:4]	0000_B: TBD nCK 0001_B: TBD nCK ... 1110_B: TBD nCK 1111_B: RFU	

Notes:
1 - tWR is currently defined as 45ns across all bins, this table will convert that value into nCK configuration options

3.5.9 MR7 (MA[7:0]=07_H) - Q2'17 Ballot #1845.31A

MR7 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]

Function	Register Type	Operand	Data	Notes

3.5.10 MR8 (MA[7:0]=08_H) - Preamble / Postamble - Q2'17 Ballot #1845.31A

MR8 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Write Postamble Settings		Read Postamble Settings		Write Preamble Settings		Read Preamble Settings	

Function	Register Type	Operand	Data	Notes
Read Preamble Settings	R/W	OP[1:0]	00_B: 1 tCK 01_B: 2 tCK 10_B: 3 tCK 11_B: Reserved	
Write Preamble Settings	R/W	OP[3:2]	00_B: 1 tCK 01_B: 2 tCK 10_B: 3 tCK 11_B: Reserved	
Read Postamble Settings	R/W	OP[5:4]	00_B: 0.5 tCK 01_B: 1.5 tCK 10_B: Reserved 11_B: Reserved	
Write Postamble Settings	R/W	OP[7:6]	00_B: 0.5 tCK 01_B: 1.5 tCK 10_B: Reserved 11_B: Reserved	

3.5.11 MR9 (MA[7:0]=09_H) - VREF Config - Q2'17 Ballot #1845.30A - w/Editorial Updates

MR9 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU						Int VREF CA Mon	Int VREF DQ Mon

Function	Register Type	Operand	Data	Notes
Int VREF DQ Mon	R/W	OP[0]	0_B: Normal (Default) 1_B: Int VREF DQ Monitor	
Int VREF CA Mon	R/W	OP[1]	0_B: Normal (Default) 1_B: Int VREF CA Monitor	
RFU	R/W	OP[7:2]	RFU	

3.5.12 MR10 (MA[7:0]=0A$_H$) - Vref DQ Calibration Settings - Q2'17 Ballot #1845.30A

MR10 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Vref DQ Cal Value							

Function	Register Type	Operand	Data	Notes
Vref DQ Cal Value	R/W	OP[7:0]	TBD	

3.5.13 MR11 (MA[7:0]=0B$_H$) - Vref CA Calibration Settings - Q2'17 Ballot #1845.30A

MR11 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Vref CA Cal Value							

Function	Register Type	Operand	Data	Notes
Vref CA Cal Value	R/W	OP[7:0]	TBD	

3.5.14 MR12 (MA [7:0] = $0C_H$) - tCCD_L - No Ballot

MR12 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
				tCCD_L			

Function	Register Type	Operand	Data	Notes
tCCD_L	R/W	OP[3:0]	RFU	

3.5.15 MR13 (MA [7:0] = $0C_H$) - Blank - No Ballot

MR13 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]

Function	Register Type	Operand	Data	Notes

3.5.16 MR14 (MA[7:0]=$0E_H$) - ECC Configuration - Q1'17 Ballot #1845.40

MR14 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
ECS Entry	ECS Reset	RFU	ECS OP[4]	ECS OP[3]	ECS OP[2]	ECS OP[1]	ECS OP[0]

Function	Register Type	Operand	Data	Notes
ECS OP[0]	R/W	OP[0]	RFU	
ECS OP[1]	R/W	OP[1]	RFU	
ECS OP[2]	R/W	OP[2]	RFU	
ECS OP[3]	R/W	OP[3]	RFU	
ECS OP[4]	R/W	OP[4]	RFU	
RFU	R/W	OP[5]	RFU	
ECS Reset	R/W	OP[6]	Reset ECC Counter	
ECS Entry	R/W	OP[7]	0_B: Normal Operation (Default) 1_B: ECS Entry	

3.5.17 MR15 (MA[7:0]=$0F_H$) - ECS Threshold - Q1'17 Ballot #1845.40

MR15 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	ECS Error Threshold					

Function	Register Type	Operand	Data	Notes
ECS Error Threshold	R/W	OP[5:0]	TBD	
RFU		OP[6]	RFU	
RFU		OP[7]	RFU	

3.5.18 MR16 (MA [7:0] = 10_H) - Reserved for Transparency 1 - Q1'17 Ballot #1845.40

MR16 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Reserved for Transparency							

Function	Register Type	Operand	Data	Notes

3.5.19 MR17 (MA [7:0] = 11_H) - Reserved for Transparency 2 - Q1'17 Ballot #1845.40

MR17 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Reserved for Transparency							

Function	Register Type	Operand	Data	Notes

3.5.20 MR18 (MA [7:0] = 12_H) - Reserved for Transparency 3 - Q1'17 Ballot #1845.40

MR18 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Reserved for Transparency							

Function	Register Type	Operand	Data	Notes

3.5.21 MR19 (MA [7:0] = 13_H) - Reserved for Transparency 4 - Q1'17 Ballot #1845.40

MR19 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Reserved for Transparency							

Function	Register Type	Operand	Data	Notes

3.5.22 MR20 (MA [7:0] = 14_H) - Reserved for Transparency 5 - Q1'17 Ballot #1845.40

MR20 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Reserved for Transparency							

Function	Register Type	Operand	Data	Notes

3.5.23 MR21 (MA [7:0] = 15_H) - Reserved for Transparency 6 - Q1'17 Ballot #1845.40

MR21 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Reserved for Transparency							

Function	Register Type	Operand	Data	Notes

3.5.24 MR22 (MA [7:0] = 16_H) - Reserved for Transparency 7 - Q1'17 Ballot #1845.40

MR22 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Reserved for Transparency							

Function	Register Type	Operand	Data	Notes

3.5.25 MR23 (MA [7:0] = 17_H) - PPR Settings - Q1'17 Ballot #1845.41

MR23 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU						sPPR	hPPR

Function	Register Type	Operand	Data	Notes
hPPR	R/W	OP[0]	0_B: Disable 1_B: Enable	
sPPR	R/W	OP[1]	0_B: Disable 1_B: Enable	
RFU	R/W	OP[7:2]	RFU	

3.5.26 MR24 (MA [7:0] = 18_H) - Blank - No Ballot

MR24 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]

Function	Register Type	Operand	Data	Notes

3.5.27 MR25 (MA[7:0]=19_H) - Read Training Mode Settings - Q1'17 Ballot #1845.42

MR25 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
					LFSR1 Pattern Option	LFSR0 Pattern Option	Read Training Pattern Format

Function	Register Type	Operand	Data	Notes
Read Training Pattern Format	R/W	OP[0]	0_B: Serial 1_B: LFSR	
LFSR0 Pattern Option	R/W	OP[1]	0_B: LFSR 1_B: Clock	
LFSR1 Pattern Option	R/W	OP[2]	0_B: LFSR 1_B: Clock	
RFU	R/W	OP[7:2]	RFU	

3.5.28 MR26 (MA[7:0]=1A$_H$) - Read Pattern Data0 / LFSR0 - Q1'17 Ballot #1845.42

MR26 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Read Training Pattern Data0 / LFSR0 Seed							

Function	Register Type	Operand	Data	Notes
Read Pattern / LFSR Seed UI 0	R/W	OP[0]	UI<7:0> data for serial mode, LFSR0 seed for LFSR mode	1
Read Pattern / LFSR Seed UI 1	R/W	OP[1]		
Read Pattern / LFSR Seed UI 2	R/W	OP[2]		
Read Pattern / LFSR Seed UI 3	R/W	OP[3]		
Read Pattern / LFSR Seed UI 4	R/W	OP[4]		
Read Pattern / LFSR Seed UI 5	R/W	OP[5]		
Read Pattern / LFSR Seed UI 6	R/W	OP[6]		
Read Pattern / LFSR Seed UI 7	R/W	OP[7]		

Note:
1 - The default value for the **Read Training Pattern Data0/LFSR0** register setting is: 0x5A.

3.5.29 MR27 (MA[7:0]=1B$_H$) - Read Pattern Data1 / LFSR1 - Q1'17 Ballot #1845.42

MR27 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Read Training Pattern Data1 / LFSR1 Seed							

Function	Register Type	Operand	Data	Notes
Read Pattern / LFSR Seed UI 8	R/W	OP[0]	UI<15:8> data for serial mode, LFSR1 seed for LFSR mode	1
Read Pattern / LFSR Seed UI 9	R/W	OP[1]		
Read Pattern / LFSR Seed UI 10	R/W	OP[2]		
Read Pattern / LFSR Seed UI 11	R/W	OP[3]		
Read Pattern / LFSR Seed UI 12	R/W	OP[4]		
Read Pattern / LFSR Seed UI 13	R/W	OP[5]		
Read Pattern / LFSR Seed UI 14	R/W	OP[6]		
Read Pattern / LFSR Seed UI 15	R/W	OP[7]		

Note:
1 - The default value for the Read Training Pattern Data1/LFSR1 register setting is: 0x3C.

3.5.30 MR28 (MA[7:0]=1C$_H$) - Read Pattern Invert DQL7:0 (DQ7:0) - Q1'17 Ballot #1845.42

MR28 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Read Training Pattern Invert DQL7:0 (DQ7:0)							

Function	Register Type	Operand	Data	Notes
DQ Invert (Lower DQ Bits)	R/W	OP[0]	DQL0 (DQ0)	1
	R/W	OP[1]	DQL1 (DQ1)	
	R/W	OP[2]	DQL2 (DQ2)	
	R/W	OP[3]	DQL3 (DQ3)	
	R/W	OP[4]	DQL4 (DQ4)	
	R/W	OP[5]	DQL5 (DQ5)	
	R/W	OP[6]	DQL6 (DQ6)	
	R/W	OP[7]	DQL7 (DQ7)	

Note:
1 - The default value for the **Read Training Pattern Invert DQL7:0 (DQ7:0)** register setting is: 0x00.

3.5.31 MR29 (MA[7:0]= D$_H$) - Read Pattern Invert DQU7:0 (DQ15:8) - Q1'17 Ballot #1845.42

MR29 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Read Training Pattern Invert DQU7:0 (DQ15:8)							

Function	Register Type	Operand	Data	Notes
DQ Invert (Upper DQ Bits)	R/W	OP[0]	DQU0 (DQ8)	1
	R/W	OP[1]	DQU1 (DQ9)	
	R/W	OP[2]	DQU2 (DQ10)	
	R/W	OP[3]	DQU3 (DQ11)	
	R/W	OP[4]	DQU4 (DQ12)	
	R/W	OP[5]	DQU5 (DQ13)	
	R/W	OP[6]	DQU6 (DQ14)	
	R/W	OP[7]	DQU7 (DQ15)	

Note:
1 - The default value for the **Read Training Pattern Invert DQU7:0 (DQ15:8)** register setting is: 0x00.

3.5.32 MR30 (MA[7:0]=$1E_H$) - Read LFSR Assignments - Q1'17 Ballot #1845.42

MR30 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQL7/ DQU7	DQL6/ DQU6	DQL5/ DQU5	DQL4/ DQU4	DQL3/ DQU3	DQL2/ DQU2	DQL1/ DQU1	DQL0/ DQU0

Function	Register Type	Operand	Data	Notes
DQL0/DQU0	R/W	OP[0]	0_B: LFSR0 1_B: LFSR1	1
DQL1/DQU1	R/W	OP[1]	0_B: LFSR0 1_B: LFSR1	
DQL2/DQU2	R/W	OP[2]	0_B: LFSR0 1_B: LFSR1	
DQL3/DQU3	R/W	OP[3]	0_B: LFSR0 1_B: LFSR1	
DQL4/DQU4	R/W	OP[4]	0_B: LFSR0 1_B: LFSR1	
DQL5/DQU5	R/W	OP[5]	0_B: LFSR0 1_B: LFSR1	
DQL6/DQU6	R/W	OP[6]	0_B: LFSR0 1_B: LFSR1	
DQL7/DQU7	R/W	OP[7]	0_B: LFSR0 1_B: LFSR1	

Note:
1 - The default value for the **Read LFSR Assignments** register setting is: 0xFE.

3.5.33 MR31 (MA[7:0]=$1F_H$) - Read Training Pattern Address - Q1'17 Ballot #1845.42

MR31 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Read Training Pattern Address							

Function	Register Type	Operand	Data	Notes
Read Training Pattern Address	R	OP[7:0]	This MR address is reserved. There are no specific register fields associated with this address. In response to the MRR to this address the DRAM will send the BL16 read training pattern. All 8 bits associated with this MR address are reserved.	

3.5.34 MR32 (MA[7:0]=20_H) - CK ODT - Q2'17 Ballot #1845.43

MR32 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU					CK ODT		

Function	Register Type	Operand	Data	Notes
CK ODT	R/W	OP[2:0]	000_B: RTT_OFF (Disable) 001_B: RZQ/0.5 (480) 010_B: RFU 011_B: RZQ/3 (80) 100_B: RFU 101_B: RFU 110_B: RZQ/6 (40) 111_B: RFU	
RFU	R/W	OP[7:3]	RFU	

3.5.35 MR33 (MA[7:0]=21_H) - CA, CS ODT - Q2'17 Ballot #1845.43 w/Editorial Update

MR33 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		CS ODT			CA ODT		

Function	Register Type	Operand	Data	Notes
CA ODT	R/W	OP[2:0]	000_B: RTT_OFF 001_B: RZQ/0.5 (480) 010_B: RZQ/1 (240) 011_B: RZQ/3 (80) 100_B: RFU 101_B: RFU 110_B: RZQ/6 (40) 111_B: RFU	
CS ODT	R/W	OP[5:3]	000_B: RTT_OFF 001_B: RZQ/0.5 (480) 010_B: RZQ/1 (240) 011_B: RZQ/3 (80) 100_B: RFU 101_B: RFU 110_B: RZQ/6 (40) 111_B: RFU	
RFU	R/W	OP[7:6]	RFU	

3.5.36 MR34 (MA[7:0]=22_H) - RTT_PARK & RTT_WR - Q2'17 Ballot #1845.43

MR34 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		RTT_WR			RTT_PARK		

Function	Register Type	Operand	Data	Notes
RTT_PARK	R/W	OP[2:0]	000_B: RTT_OFF 001_B: RZQ (240) 010_B: RZQ/2 (120) 011_B: RZQ/3 (80) 100_B: RZQ/4 (60) 101_B: RZQ/5 (48) 110_B: RZQ/6 (40) default 111_B: RFU	
RTT_WR	R/W	OP[5:3]	000_B: RTT_OFF 001_B: RZQ (240) 010_B: RZQ/2 (120) 011_B: RZQ/3 (80) 100_B: RZQ/4 (60) 101_B: RZQ/5 (48) 110_B: RZQ/6 (40) default 111_B: RFU	
RFU	TBD	OP[7:6]	RFU	

3.5.37 MR35 (MA[7:0]=23_H) - RTT_NOM_WR & RTT_NOM_RD - Q2'17 Ballot #1845.43

MR35 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		RTT_NOM_RD			RTT_NOM_WR		

Function	Register Type	Operand	Data	Notes
RTT_NOM_WR	R/W	OP[2:0]	000_B: RTT_OFF 001_B: RZQ/1 (240) 010_B: RZQ/2 (120) 011_B: RZQ/3 (80) 100_B: RZQ/4 (60) 101_B: RZQ/5 (48) 110_B: RZQ/6 (40) default 111_B: RFU	
RTT_NOM_RD	R/W	OP[5:3]	000_B: RTT_OFF 001_B: RZQ/1 (240) 010_B: RZQ/2 (120) 011_B: RZQ/3 (80) 100_B: RZQ/4 (60) 101_B: RZQ/5 (48) 110_B: RZQ/6 (40) default 111_B: RFU	
RFU	TBD	OP[6]		
ODT Control During PD	R/W	OP[7]	0_B: Disabled (Default) 1_B: Enabled	

3.5.38 MR36 (MA[7:0]= 24_H) - ODTL Write Control - Q2'17 Ballot #1845.43

MR36 Register Information

This byte is setup to allow the host controller to push out or pull in the RTT enable and disable time outside of the default setting. The default state is based on internal DRAM design. The DRAM is not responsible for inappropriate states set by the host controller using this register.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		ODTL-off_WR Sign bit	ODTLoff_WR		ODT-Lon_WR-Sign bit	ODTLon_WR	

Function	Register Type	Operand	Data	Notes
ODTLon_WR	R/W	OP[1:0]	00_B: DEFAULT 01_B: 1 Clock 10_B: 2 Clocks 11_B: TBD	1
ODTLon_WR Sign bit	R/W	OP[2]	0_B: Positive 1_B: Negative	
ODTLoff__WR	R/W	OP[4:3]	00_B: DEFAULT 01_B: 1 Clock 10_B: 2 Clocks 11_B: TBD	1
ODTLoff_WR Sign bit	R/W	OP[5]	0_B: Positive 1_B: Negative	
RFU	TBD	OP[7:6]		

NOTE:
1. Encoding using Signed bit format.

3.5.39 MR37 (MA[7:0]=25_H) - ODTL NT Write Control - Q2'17 Ballot #1845.43

MR37 Register Information

This byte is setup to allow the host controller to push out or pull in the RTT enable and disable time outside of the default setting. The default state is based on internal DRAM design. The DRAM is not responsible for inappropriate states set by the host controller using this register.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		ODTLoff_ WR_NT Sign bit	ODTLoff_WR_NT		ODTLon _WR_NT Sign bit	ODTLon_WR_NT	

Function	Register Type	Operand	Data	Notes
ODTLon_WR_NT	R/W	OP[1:0]	00_B: DEFAULT 01_B: 1 Clock 10_B: 2 Clocks 11_B: TBD	1
ODTLon_WR_NT Sign bit	R/W	OP[2]	0_B: Positive 1_B: Negative	
ODTLoff__WR_NT	R/W	OP[4:3]	00_B: DEFAULT 01_B: 1 Clock 10_B: 2 Clocks 11_B: TBD	1
ODTLoff_WR_NT Sign bit	R/W	OP[5]	0_B: Positive 1_B: Negative	
RFU	TBD	OP[7:6]		

NOTE:
1. Encoding using Signed bit format.

3.5.40 MR38 (MA[7:0]=26_H) - ODTL Read Control - Q2'17 Ballot #1845.43

MR38 Register Information

This byte is setup to allow the host controller to push out or pull in the RTT enable and disable time outside of the default setting. The default state is based on internal DRAM design. The DRAM is not responsible for inappropriate states set by the host controller using this register.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		ODTL-off_RD Sign bit	ODTLoff_RD		ODT-Lon_RD Sign bit	ODTLon_RD	

Function	Register Type	Operand	Data	Notes
ODTLon_RD	R/W	OP[1:0]	00_B: DEFAULT 01_B: 1 Clock 10_B: 2 Clocks 11_B: TBD	1
ODTLon_RD Sign bit	R/W	OP[2]	0_B: Positive 1_B: Negative	
ODTLoff_RD	R/W	OP[4:3]	00_B: DEFAULT 01_B: 1 Clock 10_B: 2 Clocks 11_B: TBD	1
ODTLoff_RD Sign bit	R/W	OP[5]	0_B: Positive 1_B: Negative	
RFU	TBD	OP[7:6]		

NOTE:
1. Encoding using Signed bit format.

3.5.41 MR39 (MA[7:0]=27_H) - ODTL NT Read Control - Q2'17 Ballot #1845.43

MR39 Register Information

This byte is setup to allow the host controller to push out or pull in the RTT enable and disable time outside of the default setting. The default state is based on internal DRAM design. The DRAM is not responsible for inappropriate states set by the host controller using this register.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		ODTL-off_RD_NT Sign bit	ODTLoff_RD_NT		ODT-Lon_RD_NT Sign bit	ODTLon_RD_NT	

Function	Register Type	Operand	Data	Notes
ODTLon_RD_NT	R/W	OP[1:0]	00_B: DEFAULT 01_B: 1 Clock 10_B: 2 Clocks 11_B: TBD	1
ODTLon_RD_NT Sign bit	R/W	OP[2]	0_B: Positive 1_B: Negative	
ODTLoff__RD_NT	R/W	OP[4:3]	00_B: DEFAULT 01_B: 1 Clock 10_B: 2 Clocks 11_B: TBD	1
ODTLoff_RD_NT Sign bit	R/W	OP[5]	0_B: Positive 1_B: Negative	
RFU	TBD	OP[7:6]		

NOTE:
1. Encoding using Signed bit format.

3.5.42 MR40 (MA[7:0]=28_H) - ODTL DQS Write Control - Q2'17 Ballot #1845.43

MR40 Register Information

This byte is setup to allow the host controller to push out or pull in the RTT enable and disable time outside of the default setting. The default state is based on internal DRAM design. The DRAM is not responsible for inappropriate states set by the host controller using this register.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		ODTLoff_DQS_WR Sign bit	ODTLoff_DQS_WR		ODTLon_DQS_WR Sign bit	ODTLon_DQS_WR	

Function	Register Type	Operand	Data	Notes
ODTLon_DQS_WR	R/W	OP[1:0]	00_B: DEFAULT 01_B: 1 Clock 10_B: 2 Clocks 11_B: TBD	1
ODTLon_DQS_WR Sign bit	R/W	OP[2]	0_B: Positive 1_B: Negative	
ODTLoff__DQS_WR	R/W	OP[4:3]	00_B: DEFAULT 01_B: 1 Clock 10_B: 2 Clocks 11_B: TBD	1
ODTLoff_DQS_WR Sign bit	R/W	OP[5]	0_B: Positive 1_B: Negative	
RFU	TBD	OP[7:6]		

NOTE:
1. Encoding using Signed bit format.

3.5.43 MR41 (MA[7:0]=29_H) - ODTL DQS NT Write Control - Q2'17 Ballot #1845.43

MR41 Register Information

This byte is setup to allow the host controller to push out or pull in the RTT enable and disable time outside of the default setting. The default state is based on internal DRAM design. The DRAM is not responsible for inappropriate states set by the host controller using this register.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		ODTLoff_DQS_WR_NT Sign bit	ODTLoff_DQS_WR_NT		ODTLon_DQS_WR_NT Sign bit	ODTLon_DQS_WR_NT	

Function	Register Type	Operand	Data	Notes
ODTLon_DQS_WR_NT	R/W	OP[1:0]	00_B: DEFAULT 01_B: 1 Clock 10_B: 2 Clocks 11_B: TBD	1
ODTLon_DQS_WR_NT Sign bit	R/W	OP[2]	0_B: Positive 1_B: Negative	
ODTLoff__DQS_WR_NT	R/W	OP[4:3]	00_B: DEFAULT 01_B: 1 Clock 10_B: 2 Clocks 11_B: TBD	1
ODTLoff_DQS_WR_NT Sign bit	R/W	OP[5]	0_B: Positive 1_B: Negative	
RFU	TBD	OP[7:6]		

NOTE:
1. Encoding using Signed bit format.

3.5.44 MR42 (MA[7:0]=$2A_H$) - ODTL DQS Read Control - Q2'17 Ballot #1845.43

MR42 Register Information

This byte is setup to allow the host controller to push out or pull in the RTT enable and disable time outside of the default setting. The default state is based on internal DRAM design. The DRAM is not responsible for inappropriate states set by the host controller using this register.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		ODTLoff_DQS_RD Sign bit	ODTLoff_DQS_RD		ODTLon_DQS_RD Sign bit	ODTLon_DQS_RD	

Function	Register Type	Operand	Data	Notes
ODTLon_DQS_RD	R/W	OP[1:0]	00_B: DEFAULT 01_B: 1 Clock 10_B: 2 Clocks 11_B: TBD	1
ODTLon_DQS_RD Sign bit	R/W	OP[2]	0_B: Positive 1_B: Negative	
ODTLoff_DQS_RD	R/W	OP[4:3]	00_B: DEFAULT 01_B: 1 Clock 10_B: 2 Clocks 11_B: TBD	1
ODTLoff_DQS_RD Sign bit	R/W	OP[5]	0_B: Positive 1_B: Negative	
RFU	TBD	OP[7:6]		

NOTE:
1. Encoding using Signed bit format.

3.5.45 MR43 (MA[7:0]=2B$_H$) - ODTL NT Read Control - Q2'17 Ballot #1845.43

MR43 Register Information

This byte is setup to allow the host controller to push out or pull in the RTT enable and disable time outside of the default setting. The default state is based on internal DRAM design. The DRAM is not responsible for inappropriate states set by the host controller using this register.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		ODTLoff_DQS_RD_NT Sign bit	ODTLoff_DQS_RD_NT		ODTLon_DQS_RD_NT Sign bit	ODTLon_DQS_RD_NT	

Function	Register Type	Operand	Data	Notes
ODTLon_DQS_RD_NT	R/W	OP[1:0]	00_B: DEFAULT 01_B: 1 Clock 10_B: 2 Clocks 11_B: TBD	1
ODTLon_DQS_RD_NT Sign bit	R/W	OP[2]	0_B: Positive 1_B: Negative	
ODTLoff_DQS_RD_NT	R/W	OP[4:3]	00_B: DEFAULT 01_B: 1 Clock 10_B: 2 Clocks 11_B: TBD	1
ODTLoff_DQS_RD_NT Sign bit	R/W	OP[5]	0_B: Positive 1_B: Negative	
RFU	TBD	OP[7:6]		

NOTE:
1. Encoding using Signed bit format.

3.5.46 MR44 (MA[7:0]=$2C_H$) - Read DQS Offset Timing - Q3'17 Ballot #1845.52 w/ Edits

MR44 Register Information

This byte is used for configuring the DRAM to support different HOST receiver designs.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU						Read DQS offset timing	

Function	Register Type	Operand	Data	Notes
Read DQS offset timing	R/W	OP[1:0]	000_B: 0 Clock (DEFAULT) 001_B: 1 Clock 010_B: 2 Clocks 011_B: 3 Clocks ~~100_B: TBD~~ ~~101_B: TBD~~ ~~110_B: TBD~~ ~~111_B: TBD~~	1
RFU	TBD	OP[7:2]	RFU	

NOTE:
1. Encoding using Signed bit format.

3.5.47 MR45 (MA[7:0]=2D$_H$) - DQS Interval Control - Q3'17 Ballot #1845.44A

MR45 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQS Interval CLK Count							DQS Interval Osc Control

Function	Register Type	Operand	Data	Notes
DQS Interval Osc Control	R/W	OP[0]	0_B: DQS Interval timer stop via MPC Command (Default) 1_B: DQS Timer stops after N clocks	
DQS Interval CLK Count	R/W	OP[7:1]	TBD - Number of Clocks to Stop	

NOTE:

3.5.48 MR46 (MA[7:0]=2E$_H$) - DQS Osc Count - LSB - Q2'17 Ballot #1845.44

MR46 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQS Oscillator Count - LSB							

Function	Register Type	Operand	Data	Notes
DQS Oscillator Count - LSB	Read Only	OP[7:0]	0 - 255 LSB DRAM DQS Oscillator Count	

NOTE:
1. MR46 reports the LSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR46 and MR47 must be read (MRR) and combined to get the value of the DQS Oscillator count.
3. A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR46/MR47.

3.5.49 MR47 (MA[7:0]=2F$_H$) - DQS Osc Count - MSB - Q2'17 Ballot #1845.44

MR47 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQS Oscillator Count - MSB							

Function	Register Type	Operand	Data	Notes
DQS Oscillator Count - MSB	Read Only	OP[7:0]	0 - 255 MSB DRAM DQS Oscillator Count	

NOTE:
1. MR47 reports the MSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR46 and MR47 must be read (MRR) and combined to get the value of the DQS Oscillator count.
3. A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR46/MR47.

3.5.50 MR48 (MA[7:0]=30_H) - Write Pattern Mode - Q2'17 Ballot #1845.45

MR48 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Write Pattern Mode							

Function	Register Type	Operand	Data	Notes
DQL0/DQU0	R/W	OP[0]	Valid	1,2
DQL1/DQU1	R/W	OP[1]		
DQL2/DQU2	R/W	OP[2]		
DQL3/DQU3	R/W	OP[3]		
DQL4/DQU4	R/W	OP[4]		
DQL5/DQU5	R/W	OP[5]		
DQL6/DQU6	R/W	OP[6]		
DQL7/DQU7	R/W	OP[7]		

NOTES:
1. OP[7:0] can be independently programmed with either "0" or "1".
2. Default is all zero's for OP[7:0]

3.5.51 MR49 (MA[7:0]=31_H) Fast Zero Init Q2'17 Ballot #1845.46

MR49 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU						Fast Zero Status	Fast Zero Entry

Function	Register Type	Operand	Data	Notes
Fast Zero Entry	W	OP[0]	0_B: Normal Operation (Default) 1_B: Enter Fast Zero Mode	
Fast Zero Status	R	OP[1]	0_B: Complete 1_B: In Progress	1, 2
RFU	TBD	OP[7:2]		

NOTES:

1 - This bit will stay as "1 - In Progress" until it has completed upon which time it will revert back to "0 - Complete".

2 - In the case of 3DS devices, this bit will stay as "1 - In Progress" until all 3DS Slices have completed upon which time it will revert back to "0 - Complete"

3.5.52 MR50 (MA[7:0]=32_H) - Write CRC Settings - Q2'17 Ballot #1845.47

MR50 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	Write CRC auto-disable status	Write CRC auto-dis-able enable	Write CRC error status	Write CRC enable upper nibble	Write CRC enable	Read CRC enable

Function	Register Type	Operand	Data	Notes
Read CRC enable	RW	OP[0]	0_B: Disable (Default) 1_B: Enable	
Write CRC enable	RW	OP[1]	0_B: Disable (Default) 1_B: Enable	
Write CRC enable upper nibble	RW	OP[2]	0_B: Disable (Default) 1_B: Enable	1
Write CRC error status	RW	OP[3]	0_B: Clear 1_B: Error	
Write CRC auto-disable enable	RW	OP[4]	0_B: Disable (Default) 1_B: Enable	
Write CRC auto-disable status	RW	OP[5]	0_B: Not triggered 1_B: Triggered	
RFU	RFU	OP[6]	RFU	
RFU	RFU	OP[7]	RFU	

NOTES:
1 - For x8 only

3.5.53 MR51 (MA[7:0]=33_H) - Write CRC Auto-Disable Threshold - Q2'17 Ballot #1845.47

MR51 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]

Function	Register Type	Operand	Data	Notes
Write CRC auto-disable threshold	RW	OP[6:0]	0000000_B: 0 ... 1111111_B: 127	
RFU	RFU	OP[7]	RFU	

3.5.54 MR52 (MA[7:0]=34_H) - Write CRC Auto-Disable Window - Q2'17 Ballot #1845.47

MR52 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]

Function	Register Type	Operand	Data	Notes
Write CRC auto-disable window	RW	OP[6:0]	0000000_B: 0 ... 1111111_B: 127	
RFU	RFU	OP[7]	RFU	

3.5.55 MR53 (MA[7:0]=35_H) - Loopback - Q3'17 Ballot #1845.61

MR53 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Loopback Termination Selection	Loopback Select Phase		Loopback Output Select				

Function	Register Type	Operand	Data
Loopback Output Select	R/W	OP[4:0]	00000_B: Loopback Disabled (Default) 00001_B: Loopback DML 00010_B: Loopback DMU 00011_B: Loopback DQL0 00100_B: Loopback DQL1 00101_B: Loopback DQL2 00110_B: Loopback DQL3 00111_B: Loopback DQL4 (X8 and X16 only) 01000_B: Loopback DQL5 (X8 and X16 only) 01001_B: Loopback DQL6 (X8 and X16 only) 01010_B: Loopback DQL7 (X8 and X16 only) 01011_B: Loopback DQU0 (X16 only) 01100_B: Loopback DQU1 (X16 only) 01101_B: Loopback DQU2 (X16 only) 01110_B: Loopback DQU3 (X16 only) 01111_B: Loopback DQU4 (X16 only) 10000_B: Loopback DQU5 (X16 only) 10001_B: Loopback DQU6 (X16 only) 10010_B: Loopback DQU7 (X16 only) 10011_B: Vendor Specific 10100_B: Vendor Specific 10101_B: RFU : 11111_B: RFU
Loopback Select Phase	R/W	OP[6:5]	00_B: Loopback Select Phase A 01_B: Loopback Select Phase B (4-way and 2-way interleave only) 10_B: Loopback Select Phase C (4-way interleave only) 11_B: Loopback Select Phase D (4-way interleave only)
Loopback Termination Selection	R/W	OP[7]	00_B: HiZ (Default) 01_B: Termination Enabled

NOTES:

1. When Loopback is disabled, both LBDQS and LBDQ pins are either at HiZ or Termination Mode per MR53 OP[7]. Loopback Termination default value is 48-ohms
2. When Loopback is enabled, both LBDQS and LBDQ pins are in driver mode using default RON of 34-ohms
3. Phase A through D selects which bit in the multiplexer is being selected for Loopback output
4. When Loopback is enabled, the termination scheme defined in MR53 OP[7] is not used

3.5.56 MR54 to MR62 - Blank - No Ballot

MR54 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]

Function	Register Type	Operand	Data	Notes

3.5.57 MR63 (MA[7:0]=3F$_H$) - DRAM Scratch Pad - Q2'17 Ballot #1845.48

MR63 Register Information

This MR is used by the host controller to read back Control Words from the RCD. Control Words are the RCD equivalent of the DRAM MR registers. The DRAM implements MR63 as a simple read/write register, writable via an MRW to address 3Fh, and readable via an MRR to address 3Fh.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DRAM Scratch Pad							

Function	Register Type	Operand	Data	Notes
DRAM Scratch Pad	R/W	**OP[7:0]**	Any value is valid	**1**

NOTE: The contents of this register have no function in the DRAM. Details for this function can be found in the DDR5 RCD01 Specification.

The following data is just for reference and is not part of the DRAM specification.

3.5.57.1 RCD Control Word Usage Example

The method to read an RCD Control Word is as follows:

- The host controller writes to the RCD's CW Read Pointer, which selects the RCD control word to be read.
- The host controller then does an MRW to DRAM MR63. This MRW passes through the RCD to the DRAMs, but is modified by the RCD. The RCD will detect this write to MR63 and replace the data from the host controller with the contents of the RCD register pointed to by the CW Read Pointer.
- The host controller will then read the DRAM's MR63, which now contains the value from the desired RCD control word. All DRAMs in the rank will return this same value to the host controller

3.5.58 MR64 to MR111 - Blank - No Ballot

MR64 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]

Function	Register Type	Operand	Data	Notes

3.5.59 Mode Register Definitions for DFE - Q3'17 Ballot #1845.62 w/Editorial Updates

(Intel prefers to compress the documentation of these byte down to only a table showing the Mode Register lists and byte definitions for VGA, Tap1, Tap2, Tap3 and Tap4)

The following mode registers are used to configure the Decision Feedback Equalization (DFE) feature of the DRAM. The Mode Registers MA[7:0]=80-FF_H are organized in a way such that mode registers for programming of DFE configuration per DQ or DM are grouped together. For example:

DQL0 starts at MA[7:0]=80_H,
DQL1 starts at MA[7:0]=88_H,
:
DQU6 starts at MA[7:0]=$F0_H$,
DQU7 starts at MA[7:0]=$F8_H$

Looking further into the 8-bit binary encoding, MA[6:3] is defined as a direct mapping for DQL0 to DQU7, i.e.,

MA[7:0]=1000:0XXXb for DQ0,
MA[7:0]=1000:1XXXb for DQ1,
:
MA[7:0]=1111:0XXXb for DQU6
MA[7:0]=1111:1XXXb for DQU7.

3.5.60 MR112 (MA[7:0]=70_H) - DML DFE VGA - Q3'17 Ballot #1845.62

MR112 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	RFU	RFU	Sign Bit	DML DFE Gain Bias		

Function	Register Type	Operand	Data	Notes
DML DFE Gain Bias	R/W	OP[2:0]	111_B: RFU 101_B: RFU 100_B: RFU 011_B: DFE Gain Bias Step +3 010_B: DFE Gain Bias Step +2 001_B: DFE Gain Bias Step +1 000_B: DFE Gain Bias Step +0 (Default)	1,2,3
Sign Bit DML Gain Bias	R/W	OP[3]	0_B: Positive DFE Gain Bias (Default) 1_B: Negative DFE Gain Bias	
RFU	R/W	OP[7:4]	RFU	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.61 MR113 (MA[7:0]=71_H) - DML DFE Tap-1 - Q3'17 Ballot #1845.62

MR113 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DML DFE Tap-1 Bias Programming					

Function	Register Type	Operand	Data	Notes
DML DFE Tap-1 Bias	R/W	OP[5:0]	111111_B: RFU : 101001_B: RFU 101000_B: DFE Tap-1 Bias Step +40 100110_B: DFE Tap-1 Bias Step +39 100101_B: DFE Tap-1 Bias Step +38 : 000101_B: DFE Tap-1 Bias Step +5 000100_B: DFE Tap-1 Bias Step +4 000011_B: DFE Tap-1 Bias Step +3 000010_B: DFE Tap-1 Bias Step +2 000001_B: DFE Tap-1 Bias Step +1 000000_B: DFE Tap-1 Bias Step +0 (Default)	1,2,3
Sign Bit DML DFE Tap-1 Bias	R/W	OP[6]	0_B: Positive DFE Tap-1 Bias (Default) 1_B: Negative DFE Tap-1 Bias	
Enable/Disable DML DFE Tap-1	R/W	OP[7]	0_B: DFE Tap-1 Disable (Default) 1_B: DFE Tap-1 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.62 MR114 (MA[7:0]=72_H) - DML DFE Tap-2 - Q3'17 Ballot #1845.62

MR114 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DML DFE Tap-2 Bias Programming					

Function	Register Type	Operand	Data	Notes
DML DFE Tap-2 Bias	R/W	OP[5:0]	111111_B: RFU : 010000_B: RFU 001111_B: DFE Tap-2 Bias Step +15 001110_B: DFE Tap-2 Bias Step +14 001011_B: DFE Tap-2 Bias Step +13 : 000101_B: DFE Tap-2 Bias Step +5 000100_B: DFE Tap-2 Bias Step +4 000011_B: DFE Tap-2 Bias Step +3 000010_B: DFE Tap-2 Bias Step +2 000001_B: DFE Tap-2 Bias Step +1 000000_B: DFE Tap-2 Bias Step +0 (Default)	1,2,3
Sign Bit DML DFE Tap-2 Bias	R/W	OP[6]	0_B: Positive DFE Tap-2 Bias (Default) 1_B: Negative DFE Tap-2 Bias	
Enable/Disable DML DFE Tap-2	R/W	OP[7]	0_B: DFE Tap-2 Disable (Default) 1_B: DFE Tap-2 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.63 MR115 (MA[7:0]=73_H) - DML DFE Tap-3 - Q3'17 Ballot #1845.62

MR115 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DML DFE Tap-3 Bias Programming					

Function	Register Type	Operand	Data	Notes
DML DFE Tap-3 Bias	R/W	OP[5:0]	111111_B: RFU : 001011_B: RFU 001010_B: DFE Tap-3 Bias Step +12 001011_B: DFE Tap-3 Bias Step +11 001010_B: DFE Tap-3 Bias Step +10 : 000101_B: DFE Tap-3 Bias Step +5 000100_B: DFE Tap-3 Bias Step +4 000011_B: DFE Tap-3 Bias Step +3 000010_B: DFE Tap-3 Bias Step +2 000001_B: DFE Tap-3 Bias Step +1 000000_B: DFE Tap-3 Bias Step +0 (Default)	1,2,3
Sign Bit DML DFE Tap-3 Bias	R/W	OP[6]	0_B: Positive DFE Tap-3 Bias (Default) 1_B: Negative DFE Tap-3 Bias	
Enable/Disable DML DFE Tap-3	R/W	OP[7]	0_B: DFE Tap-3 Disable (Default) 1_B: DFE Tap-3 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.64 MR116 (MA[7:0]=74_H) - DML DFE Tap-4 - Q3'17 Ballot #1845.62

MR116 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DML DFE Tap-4 Bias Programming					

Function	Register Type	Operand	Data	Notes
DML DFE Tap-4 Bias	R/W	OP[5:0]	111111_B: RFU : 001001_B: RFU 001000_B: DFE Tap-4 Bias Step +8 000111_B: DFE Tap-4 Bias Step +7 000110_B: DFE Tap-4 Bias Step +6 000101_B: DFE Tap-4 Bias Step +5 000100_B: DFE Tap-4 Bias Step +4 000011_B: DFE Tap-4 Bias Step +3 000010_B: DFE Tap-4 Bias Step +2 000001_B: DFE Tap-4 Bias Step +1 000000_B: DFE Tap-4 Bias Step +0 (Default)	1,2,3
Sign Bit DML DFE Tap-4 Bias	R/W	OP[6]	0_B: Positive DFE Tap-4 Bias (Default) 1_B: Negative DFE Tap-4 Bias	
Enable/Disable DML DFE Tap-4	R/W	OP[7]	0_B: DFE Tap-4 Disable (Default) 1_B: DFE Tap-4 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.65 MR117 through MR119 are undefined.

There a currently no plans to utilize these addresses.

3.5.66 MR120 (MA[7:0]=78_H) - DMU DFE VGA - Q3'17 Ballot #1845.62

MR120 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	RFU	RFU	Sign Bit	DMU DFE Gain Bias		

Function	Register Type	Operand	Data	Notes
DMU DFE Gain Bias	R/W	OP[2:0]	111_B: RFU 101_B: RFU 100_B: RFU 011_B: DFE Gain Bias Step +3 010_B: DFE Gain Bias Step +2 001_B: DFE Gain Bias Step +1 000_B: DFE Gain Bias Step +0 (Default)	1,2,3
Sign Bit DMU Gain Bias	R/W	OP[3]	0_B: Positive DFE Gain Bias (Default) 1_B: Negative DFE Gain Bias	
RFU	R/W	OP[7:4]	RFU	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.67 MR121 (MA[7:0]=79_H) - DMU DFE Tap-1 - Q3'17 Ballot #1845.62

MR121 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	RFU	DMU DFE Tap-1 Bias Programming					

Function	Register Type	Operand	Data	Notes
DMU DFE Tap-1 Bias	R/W	OP[5:0]	111111_B: RFU : 101001_B: RFU 101000_B: DFE Tap-1 Bias Step +40 100110_B: DFE Tap-1 Bias Step +39 100101_B: DFE Tap-1 Bias Step +38 : 000101_B: DFE Tap-1 Bias Step +5 000100_B: DFE Tap-1 Bias Step +4 000011_B: DFE Tap-1 Bias Step +3 000010_B: DFE Tap-1 Bias Step +2 000001_B: DFE Tap-1 Bias Step +1 000000_B: DFE Tap-1 Bias Step +0 (Default)	1,2,3
Sign Bit DMU DFE Tap-1 Bias	R/W	OP[6]	0_B: Positive DFE Tap-1 Bias (Default) 1_B: Negative DFE Tap-1 Bias	
Enable/Disable DMU DFE Tap-1	R/W	OP[7]	0_B: DFE Tap-1 Disable (Default) 1_B: DFE Tap-1 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.68 MR122 (MA[7:0]=$7A_H$) - DMU DFE Tap-2 - Q3'17 Ballot #1845.62

MR122 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DMU DFE Tap-2 Bias Programming					

Function	Register Type	Operand	Data	Notes
DMU DFE Tap-2 Bias	R/W	OP[5:0]	111111_B: RFU : 010000_B: RFU 001111_B: DFE Tap-2 Bias Step +15 001110_B: DFE Tap-2 Bias Step +14 001011_B: DFE Tap-2 Bias Step +13 : 000101_B: DFE Tap-2 Bias Step +5 000100_B: DFE Tap-2 Bias Step +4 000011_B: DFE Tap-2 Bias Step +3 000010_B: DFE Tap-2 Bias Step +2 000001_B: DFE Tap-2 Bias Step +1 000000_B: DFE Tap-2 Bias Step +0 (Default)	1,2,3
Sign Bit DMU DFE Tap-2 Bias	R/W	OP[6]	0_B: Positive DFE Tap-2 Bias (Default) 1_B: Negative DFE Tap-2 Bias	
Enable/Disable DMU DFE Tap-2	R/W	OP[7]	0_B: DFE Tap-2 Disable (Default) 1_B: DFE Tap-2 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.69 MR123 (MA[7:0]=$7B_H$) - DMU DFE Tap-3 - Q3'17 Ballot #1845.62

MR123 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DMU DFE Tap-3 Bias Programming					

Function	Register Type	Operand	Data	Notes
DMU DFE Tap-3 Bias	R/W	OP[5:0]	111111_B: RFU : 001011_B: RFU 001010_B: DFE Tap-3 Bias Step +12 001011_B: DFE Tap-3 Bias Step +11 001010_B: DFE Tap-3 Bias Step +10 : 000101_B: DFE Tap-3 Bias Step +5 000100_B: DFE Tap-3 Bias Step +4 000011_B: DFE Tap-3 Bias Step +3 000010_B: DFE Tap-3 Bias Step +2 000001_B: DFE Tap-3 Bias Step +1 000000_B: DFE Tap-3 Bias Step +0 (Default)	1,2,3
Sign Bit DMU DFE Tap-3 Bias	R/W	OP[6]	0_B: Positive DFE Tap-3 Bias (Default) 1_B: Negative DFE Tap-3 Bias	
Enable/Disable DMU DFE Tap-3	R/W	OP[7]	0_B: DFE Tap-3 Disable (Default) 1_B: DFE Tap-3 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.70 MR124 (MA[7:0]=7C$_H$) - DMU DFE Tap-4 - Q3'17 Ballot #1845.62

MR124 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DMU DFE Tap-4 Bias Programming					

Function	Register Type	Operand	Data	Notes
DMU DFE Tap-4 Bias	R/W	OP[5:0]	111111_B: RFU : 001001_B: RFU 001000_B: DFE Tap-4 Bias Step +8 000111_B: DFE Tap-4 Bias Step +7 000110_B: DFE Tap-4 Bias Step +6 000101_B: DFE Tap-4 Bias Step +5 000100_B: DFE Tap-4 Bias Step +4 000011_B: DFE Tap-4 Bias Step +3 000010_B: DFE Tap-4 Bias Step +2 000001_B: DFE Tap-4 Bias Step +1 000000_B: DFE Tap-4 Bias Step +0 (Default)	1,2,3
Sign Bit DMU DFE Tap-4 Bias	R/W	OP[6]	0_B: Positive DFE Tap-4 Bias (Default) 1_B: Negative DFE Tap-4 Bias	
Enable/Disable DMU DFE Tap-4	R/W	OP[7]	0_B: DFE Tap-4 Disable (Default) 1_B: DFE Tap-4 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.71 MR125 through MR127 are undefined.

There a currently no plans to utilize these addresses.

3.5.72 MR128 (MA[7:0]=80_H) - DQL0 DFE VGA - Q3'17 Ballot #1845.62

MR128 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	RFU	RFU	Sign Bit	DQL0 DFE Gain Bias		

Function	Register Type	Operand	Data	Notes
DQL0 DFE Gain Bias	R/W	OP[2:0]	111_B: RFU 101_B: RFU 100_B: RFU 011_B: DFE Gain Bias Step +3 010_B: DFE Gain Bias Step +2 001_B: DFE Gain Bias Step +1 000_B: DFE Gain Bias Step +0 (Default)	1,2,3
Sign Bit DQL0 DFE Gain Bias	R/W	OP[3]	0_B: Positive DFE Gain Bias (Default) 1_B: Negative DFE Gain Bias	
RFU	R/W	OP[7:4]	RFU	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.73 MR129 (MA[7:0]=81_H) - DQL0 DFE Tap-1 - Q3'17 Ballot #1845.62

MR129 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	RFU	DQL0 DFE Tap-1 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL0 DFE Tap-1 Bias	R/W	OP[5:0]	111111_B: RFU : 101001_B: RFU 101000_B: DFE Tap-1 Bias Step +40 100110_B: DFE Tap-1 Bias Step +39 100101_B: DFE Tap-1 Bias Step +38 : 000101_B: DFE Tap-1 Bias Step +5 000100_B: DFE Tap-1 Bias Step +4 000011_B: DFE Tap-1 Bias Step +3 000010_B: DFE Tap-1 Bias Step +2 000001_B: DFE Tap-1 Bias Step +1 000000_B: DFE Tap-1 Bias Step +0 (Default)	1,2,3
Sign Bit DQL0 DFE Tap-1 Bias	R/W	OP[6]	0_B: Positive DFE Tap-1 Bias (Default) 1_B: Negative DFE Tap-1 Bias	
Enable/Disable DQL0 DFE Tap-1	R/W	OP[7]	0_B: DFE Tap-1 Disable (Default) 1_B: DFE Tap-1 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.74 MR130 (MA[7:0]=82_H) - DQL0 DFE Tap-2 - Q3'17 Ballot #1845.62

MR130 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQL0 DFE Tap-2 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL0 DFE Tap-2 Bias	R/W	OP[5:0]	111111_B: RFU : 010000_B: RFU 001111_B: DFE Tap-2 Bias Step +15 001110_B: DFE Tap-2 Bias Step +14 001011_B: DFE Tap-2 Bias Step +13 : 000101_B: DFE Tap-2 Bias Step +5 000100_B: DFE Tap-2 Bias Step +4 000011_B: DFE Tap-2 Bias Step +3 000010_B: DFE Tap-2 Bias Step +2 000001_B: DFE Tap-2 Bias Step +1 000000_B: DFE Tap-2 Bias Step +0 (Default)	1,2,3
Sign Bit DQL0 DFE Tap-2 Bias	R/W	OP[6]	0_B: Positive DFE Tap-2 Bias (Default) 1_B: Negative DFE Tap-2 Bias	
Enable/Disable DQL0 DFE Tap-2	R/W	OP[7]	0_B: DFE Tap-2 Disable (Default) 1_B: DFE Tap-2 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.75 MR131 (MA[7:0]=83_H) - DQL0 DFE Tap-3 - Q3'17 Ballot #1845.62

MR131 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQL0 DFE Tap-3 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL0 DFE Tap-3 Bias	R/W	OP[5:0]	111111_B: RFU : 001011_B: RFU 001010_B: DFE Tap-3 Bias Step +12 001011_B: DFE Tap-3 Bias Step +11 001010_B: DFE Tap-3 Bias Step +10 : 000101_B: DFE Tap-3 Bias Step +5 000100_B: DFE Tap-3 Bias Step +4 000011_B: DFE Tap-3 Bias Step +3 000010_B: DFE Tap-3 Bias Step +2 000001_B: DFE Tap-3 Bias Step +1 000000_B: DFE Tap-3 Bias Step +0 (Default)	1,2,3
Sign Bit DQL0 DFE Tap-3 Bias	R/W	OP[6]	0_B: Positive DFE Tap-3 Bias (Default) 1_B: Negative DFE Tap-3 Bias	
Enable/Disable DQL0 DFE Tap-3	R/W	OP[7]	0_B: DFE Tap-3 Disable (Default) 1_B: DFE Tap-3 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.76 MR132 (MA[7:0]=84_H) - DQL0 DFE Tap-4 - Q3'17 Ballot #1845.62

MR132 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQL0 DFE Tap-4 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL0 DFE Tap-4 Bias	R/W	OP[5:0]	111111_B: RFU : 001001_B: RFU 001000_B: DFE Tap-4 Bias Step +8 000111_B: DFE Tap-4 Bias Step +7 000110_B: DFE Tap-4 Bias Step +6 000101_B: DFE Tap-4 Bias Step +5 000100_B: DFE Tap-4 Bias Step +4 000011_B: DFE Tap-4 Bias Step +3 000010_B: DFE Tap-4 Bias Step +2 000001_B: DFE Tap-4 Bias Step +1 000000_B: DFE Tap-4 Bias Step +0 (Default)	1,2,3
Sign Bit DQL0 DFE Tap-4 Bias	R/W	OP[6]	0_B: Positive DFE Tap-4 Bias (Default) 1_B: Negative DFE Tap-4 Bias	
Enable/Disable DQL0 DFE Tap-4	R/W	OP[7]	0_B: DFE Tap-4 Disable (Default) 1_B: DFE Tap-4 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.77 MR133 through MR135 are undefined.

There a currently no plans to utilize these addresses.

3.5.78 MR136 (MA[7:0]=88_H) - DQL1 DFE VGA - Q3'17 Ballot #1845.62

MR136 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	RFU	RFU	Sign Bit	DQL1 DFE Gain Bias		

Function	Register Type	Operand	Data	Notes
DQL1 DFE Gain Bias	R/W	OP[2:0]	111_B: RFU 101_B: RFU 100_B: RFU 011_B: DFE Gain Bias Step +3 010_B: DFE Gain Bias Step +2 001_B: DFE Gain Bias Step +1 000_B: DFE Gain Bias Step +0 (Default)	1,2,3
Sign Bit DQL1 Gain Bias	R/W	OP[3]	0_B: Positive DFE Gain Bias (Default) 1_B: Negative DFE Gain Bias	
RFU	R/W	OP[7:4]	RFU	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.79 MR137 (MA[7:0]=89_H) - DQL1 DFE Tap-1- Q3'17 Ballot #1845.62

MR137 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	RFU	DQL1 DFE Tap-1 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL1 DFE Tap-1 Bias	R/W	OP[5:0]	111111_B: RFU : 101001_B: RFU 101000_B: DFE Tap-1 Bias Step +40 100110_B: DFE Tap-1 Bias Step +39 100101_B: DFE Tap-1 Bias Step +38 : 000101_B: DFE Tap-1 Bias Step +5 000100_B: DFE Tap-1 Bias Step +4 000011_B: DFE Tap-1 Bias Step +3 000010_B: DFE Tap-1 Bias Step +2 000001_B: DFE Tap-1 Bias Step +1 000000_B: DFE Tap-1 Bias Step +0 (Default)	1,23
Sign Bit DQL1 DFE Tap-1 Bias	R/W	OP[6]	0_B: Positive DFE Tap-1 Bias (Default) 1_B: Negative DFE Tap-1 Bias	
Enable/Disable DQL1 DFE Tap-1	R/W	OP[7]	0_B: DFE Tap-1 Disable (Default) 1_B: DFE Tap-1 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.80 MR138 (MA[7:0]=$8A_H$) - DQL1 DFE Tap-2 - Q3'17 Ballot #1845.62

MR138 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQL1 DFE Tap-2 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL1 DFE Tap-2 Bias	R/W	OP[5:0]	111111_B: RFU : 010000_B: RFU 001111_B: DFE Tap-2 Bias Step +15 001110_B: DFE Tap-2 Bias Step +14 001011_B: DFE Tap-2 Bias Step +13 : 000101_B: DFE Tap-2 Bias Step +5 000100_B: DFE Tap-2 Bias Step +4 000011_B: DFE Tap-2 Bias Step +3 000010_B: DFE Tap-2 Bias Step +2 000001_B: DFE Tap-2 Bias Step +1 000000_B: DFE Tap-2 Bias Step +0 (Default)	1,2,3
Sign Bit DQL1 DFE Tap-2 Bias	R/W	OP[6]	0_B: Positive DFE Tap-2 Bias (Default) 1_B: Negative DFE Tap-2 Bias	
Enable/Disable DQL1 DFE Tap-2	R/W	OP[7]	0_B: DFE Tap-2 Disable (Default) 1_B: DFE Tap-2 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.81 MR139 (MA[7:0]=$8B_H$) - DQL1 DFE Tap-3 - Q3'17 Ballot #1845.62

MR139 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQL1 DFE Tap-3 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL1 DFE Tap-3 Bias	R/W	OP[5:0]	111111_B: RFU : 001011_B: RFU 001010_B: DFE Tap-3 Bias Step +12 001011_B: DFE Tap-3 Bias Step +11 001010_B: DFE Tap-3 Bias Step +10 : 000101_B: DFE Tap-3 Bias Step +5 000100_B: DFE Tap-3 Bias Step +4 000011_B: DFE Tap-3 Bias Step +3 000010_B: DFE Tap-3 Bias Step +2 000001_B: DFE Tap-3 Bias Step +1 000000_B: DFE Tap-3 Bias Step +0 (Default)	1,2,3
Sign Bit DQL1 DFE Tap-3 Bias	R/W	OP[6]	0_B: Positive DFE Tap-3 Bias (Default) 1_B: Negative DFE Tap-3 Bias	
Enable/Disable DQL1 DFE Tap-3	R/W	OP[7]	0_B: DFE Tap-3 Disable (Default) 1_B: DFE Tap-3 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.82 MR140 (MA[7:0]=8C$_H$) - DQL1 DFE Tap-4 - Q3'17 Ballot #1845.62

MR140 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQL1 DFE Tap-4 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL1 DFE Tap-4 Bias	R/W	OP[5:0]	111111_B: RFU : 001001_B: RFU 001000_B: DFE Tap-4 Bias Step +8 000111_B: DFE Tap-4 Bias Step +7 000110_B: DFE Tap-4 Bias Step +6 000101_B: DFE Tap-4 Bias Step +5 000100_B: DFE Tap-4 Bias Step +4 000011_B: DFE Tap-4 Bias Step +3 000010_B: DFE Tap-4 Bias Step +2 000001_B: DFE Tap-4 Bias Step +1 000000_B: DFE Tap-4 Bias Step +0 (Default)	1,2,3
Sign Bit DQL1 DFE Tap-4 Bias	R/W	OP[6]	0_B: Positive DFE Tap-4 Bias (Default) 1_B: Negative DFE Tap-4 Bias	
Enable/Disable DQL1 DFE Tap-4	R/W	OP[7]	0_B: DFE Tap-4 Disable (Default) 1_B: DFE Tap-4 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.83 MR141 through MR143 are undefined.

There a currently no plans to utilize these addresses.

3.5.84 MR144 (MA[7:0]=90_H) - DQL2 DFE VGA - Q3'17 Ballot #1845.62

MR144 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	RFU	RFU	Sign Bit	DQL2 DFE Gain Bias		

Function	Register Type	Operand	Data	Notes
DQL2 DFE Gain Bias	R/W	OP[2:0]	111_B: RFU 101_B: RFU 100_B: RFU 011_B: DFE Gain Bias Step +3 010_B: DFE Gain Bias Step +2 001_B: DFE Gain Bias Step +1 000_B: DFE Gain Bias Step +0 (Default)	1,2,3
Sign Bit DQL2 DFE Gain Bias	R/W	OP[3]	0_B: Positive DFE Gain Bias (Default) 1_B: Negative DFE Gain Bias	
RFU	R/W	OP[7:4]	RFU	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.85 MR145 (MA[7:0]=91_H) - DQL2 DFE Tap-1 - Q3'17 Ballot #1845.62

MR145 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	RFU	DQL2 DFE Tap-1 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL2 DFE Tap-1 Bias	R/W	OP[5:0]	111111_B: RFU : 101001_B: RFU 101000_B: DFE Tap-1 Bias Step +40 100110_B: DFE Tap-1 Bias Step +39 100101_B: DFE Tap-1 Bias Step +38 : 000101_B: DFE Tap-1 Bias Step +5 000100_B: DFE Tap-1 Bias Step +4 000011_B: DFE Tap-1 Bias Step +3 000010_B: DFE Tap-1 Bias Step +2 000001_B: DFE Tap-1 Bias Step +1 000000_B: DFE Tap-1 Bias Step +0 (Default)	1,2,3
Sign Bit DQL2 DFE Tap-1 Bias	R/W	OP[6]	0_B: Positive DFE Tap-1 Bias (Default) 1_B: Negative DFE Tap-1 Bias	
Enable/Disable DQL2 DFE Tap-1	R/W	OP[7]	0_B: DFE Tap-1 Disable (Default) 1_B: DFE Tap-1 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.86 MR146 (MA[7:0]=92_H) - DQL2 DFE Tap-2 - Q3'17 Ballot #1845.62

MR146 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQL2 DFE Tap-2 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL2 DFE Tap-2 Bias	R/W	OP[5:0]	111111_B: RFU : 010000_B: RFU 001111_B: DFE Tap-2 Bias Step +15 001110_B: DFE Tap-2 Bias Step +14 001011_B: DFE Tap-2 Bias Step +13 : 000101_B: DFE Tap-2 Bias Step +5 000100_B: DFE Tap-2 Bias Step +4 000011_B: DFE Tap-2 Bias Step +3 000010_B: DFE Tap-2 Bias Step +2 000001_B: DFE Tap-2 Bias Step +1 000000_B: DFE Tap-2 Bias Step +0 (Default)	1,2,3
Sign Bit DQL2 DFE Tap-2 Bias	R/W	OP[6]	0_B: Positive DFE Tap-2 Bias (Default) 1_B: Negative DFE Tap-2 Bias	
Enable/Disable DQL2 DFE Tap-2	R/W	OP[7]	0_B: DFE Tap-2 Disable (Default) 1_B: DFE Tap-2 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.87 MR147 (MA[7:0]=93_H) - DQL2 DFE Tap-3 - Q3'17 Ballot #1845.62

MR147 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQL2 DFE Tap-3 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL2 DFE Tap-3 Bias	R/W	OP[5:0]	111111_B: RFU : 001011_B: RFU 001010_B: DFE Tap-3 Bias Step +12 001011_B: DFE Tap-3 Bias Step +11 001010_B: DFE Tap-3 Bias Step +10 : 000101_B: DFE Tap-3 Bias Step +5 000100_B: DFE Tap-3 Bias Step +4 000011_B: DFE Tap-3 Bias Step +3 000010_B: DFE Tap-3 Bias Step +2 000001_B: DFE Tap-3 Bias Step +1 000000_B: DFE Tap-3 Bias Step +0 (Default)	1,2,3
Sign Bit DQL2 DFE Tap-3 Bias	R/W	OP[6]	0_B: Positive DFE Tap-3 Bias (Default) 1_B: Negative DFE Tap-3 Bias	
Enable/Disable DQL2 DFE Tap-3	R/W	OP[7]	0_B: DFE Tap-3 Disable (Default) 1_B: DFE Tap-3 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.88 MR148 (MA[7:0]=94_H) - DQL2 DFE Tap-4 - Q3'17 Ballot #1845.62

MR148 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQL2 DFE Tap-4 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL2 DFE Tap-4 Bias	R/W	OP[5:0]	111111_B: RFU : 001001_B: RFU 001000_B: DFE Tap-4 Bias Step +8 000111_B: DFE Tap-4 Bias Step +7 000110_B: DFE Tap-4 Bias Step +6 000101_B: DFE Tap-4 Bias Step +5 000100_B: DFE Tap-4 Bias Step +4 000011_B: DFE Tap-4 Bias Step +3 000010_B: DFE Tap-4 Bias Step +2 000001_B: DFE Tap-4 Bias Step +1 000000_B: DFE Tap-4 Bias Step +0 (Default)	1,2,3
Sign Bit DQL2 DFE Tap-4 Bias	R/W	OP[6]	0_B: Positive DFE Tap-4 Bias (Default) 1_B: Negative DFE Tap-4 Bias	
Enable/Disable DQL2 DFE Tap-4	R/W	OP[7]	0_B: DFE Tap-4 Disable (Default) 1_B: DFE Tap-4 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.89 MR149 through MR151 are undefined.

There a currently no plans to utilize these addresses.

3.5.90 MR152 (MA[7:0]=98_H) - DQL3 DFE VGA - Q3'17 Ballot #1845.62

MR152 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	RFU	RFU	Sign Bit	DQL3 DFE Gain Bias		

Function	Register Type	Operand	Data	Notes
DQL3 DFE Gain Bias	R/W	OP[2:0]	111_B: RFU 101_B: RFU 100_B: RFU 011_B: DFE Gain Bias Step +3 010_B: DFE Gain Bias Step +2 001_B: DFE Gain Bias Step +1 000_B: DFE Gain Bias Step +0 (Default)	1,2,3
Sign Bit DQL3 Gain Bias	R/W	OP[3]	0_B: Positive DFE Gain Bias (Default) 1_B: Negative DFE Gain Bias	
RFU	R/W	OP[7:4]	RFU	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.91 MR153 (MA[7:0]=99_H) - DQL3 DFE Tap-1 - Q3'17 Ballot #1845.62

MR153 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	RFU	DQL3 DFE Tap-1 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL3 DFE Tap-1 Bias	R/W	OP[5:0]	111111_B: RFU : 101001_B: RFU 101000_B: DFE Tap-1 Bias Step +40 100110_B: DFE Tap-1 Bias Step +39 100101_B: DFE Tap-1 Bias Step +38 : 000101_B: DFE Tap-1 Bias Step +5 000100_B: DFE Tap-1 Bias Step +4 000011_B: DFE Tap-1 Bias Step +3 000010_B: DFE Tap-1 Bias Step +2 000001_B: DFE Tap-1 Bias Step +1 000000_B: DFE Tap-1 Bias Step +0 (Default)	1,2,3
Sign Bit DQL3 DFE Tap-1 Bias	R/W	OP[6]	0_B: Positive DFE Tap-1 Bias (Default) 1_B: Negative DFE Tap-1 Bias	
Enable/Disable DQL3 DFE Tap-1	R/W	OP[7]	0_B: DFE Tap-1 Disable (Default) 1_B: DFE Tap-1 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.92 MR154 (MA[7:0]=$9A_H$) - DQL3 DFE Tap-2 - Q3'17 Ballot #1845.62

MR154 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQL3 DFE Tap-2 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL3 DFE Tap-2 Bias	R/W	OP[5:0]	111111_B: RFU : 010000_B: RFU 001111_B: DFE Tap-2 Bias Step +15 001110_B: DFE Tap-2 Bias Step +14 001011_B: DFE Tap-2 Bias Step +13 : 000101_B: DFE Tap-2 Bias Step +5 000100_B: DFE Tap-2 Bias Step +4 000011_B: DFE Tap-2 Bias Step +3 000010_B: DFE Tap-2 Bias Step +2 000001_B: DFE Tap-2 Bias Step +1 000000_B: DFE Tap-2 Bias Step +0 (Default)	1,2,3
Sign Bit DQL3 DFE Tap-2 Bias	R/W	OP[6]	0_B: Positive DFE Tap-2 Bias (Default) 1_B: Negative DFE Tap-2 Bias	
Enable/Disable DQL3 DFE Tap-2	R/W	OP[7]	0_B: DFE Tap-2 Disable (Default) 1_B: DFE Tap-2 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.93 MR155 (MA[7:0]=9B$_H$) - DQL3 DFE Tap-3 - Q3'17 Ballot #1845.62

MR155 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQL3 DFE Tap-3 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL3 DFE Tap-3 Bias	R/W	OP[5:0]	111111_B: RFU : 001011_B: RFU 001010_B: DFE Tap-3 Bias Step +12 001011_B: DFE Tap-3 Bias Step +11 001010_B: DFE Tap-3 Bias Step +10 : 000101_B: DFE Tap-3 Bias Step +5 000100_B: DFE Tap-3 Bias Step +4 000011_B: DFE Tap-3 Bias Step +3 000010_B: DFE Tap-3 Bias Step +2 000001_B: DFE Tap-3 Bias Step +1 000000_B: DFE Tap-3 Bias Step +0 (Default)	1,2,3
Sign Bit DQL3 DFE Tap-3 Bias	R/W	OP[6]	0_B: Positive DFE Tap-3 Bias (Default) 1_B: Negative DFE Tap-3 Bias	
Enable/Disable DQL3 DFE Tap-3	R/W	OP[7]	0_B: DFE Tap-3 Disable (Default) 1_B: DFE Tap-3 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.94 MR156 (MA[7:0]=9C$_H$) - DQL3 DFE Tap-4 - Q3'17 Ballot #1845.62

MR156 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQL3 DFE Tap-4 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL3 DFE Tap-4 Bias	R/W	OP[5:0]	111111_B: RFU : 001001_B: RFU 001000_B: DFE Tap-4 Bias Step +8 000111_B: DFE Tap-4 Bias Step +7 000110_B: DFE Tap-4 Bias Step +6 000101_B: DFE Tap-4 Bias Step +5 000100_B: DFE Tap-4 Bias Step +4 000011_B: DFE Tap-4 Bias Step +3 000010_B: DFE Tap-4 Bias Step +2 000001_B: DFE Tap-4 Bias Step +1 000000_B: DFE Tap-4 Bias Step +0 (Default)	1,2,3
Sign Bit DQL3 DFE Tap-4 Bias	R/W	OP[6]	0_B: Positive DFE Tap-4 Bias (Default) 1_B: Negative DFE Tap-4 Bias	
Enable/Disable DQL3 DFE Tap-4	R/W	OP[7]	0_B: DFE Tap-4 Disable (Default) 1_B: DFE Tap-4 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.95 MR157 through MR159 are undefined.

There a currently no plans to utilize these addresses.

3.5.96 MR160 (MA[7:0]=$A0_H$) - DQL4 DFE VGA - Q3'17 Ballot #1845.62

MR160 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	RFU	RFU	Sign Bit	DQL4 DFE Gain Bias		

Function	Register Type	Operand	Data	Notes
DQL4 DFE Gain Bias	R/W	OP[2:0]	111_B: RFU 101_B: RFU 100_B: RFU 011_B: DFE Gain Bias Step +3 010_B: DFE Gain Bias Step +2 001_B: DFE Gain Bias Step +1 000_B: DFE Gain Bias Step +0 (Default)	1,2,3
Sign Bit DQL4 DFE Gain Bias	R/W	OP[3]	0_B: Positive DFE Gain Bias (Default) 1_B: Negative DFE Gain Bias	
RFU	R/W	OP[7:4]	RFU	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.97 MR161 (MA[7:0]=$A1_H$) - DQL4 DFE Tap-1 - Q3'17 Ballot #1845.62

MR161 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	RFU	DQL4 DFE Tap-1 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL4 DFE Tap-1 Bias	R/W	OP[5:0]	111111_B: RFU : 101001_B: RFU 101000_B: DFE Tap-1 Bias Step +40 100110_B: DFE Tap-1 Bias Step +39 100101_B: DFE Tap-1 Bias Step +38 : 000101_B: DFE Tap-1 Bias Step +5 000100_B: DFE Tap-1 Bias Step +4 000011_B: DFE Tap-1 Bias Step +3 000010_B: DFE Tap-1 Bias Step +2 000001_B: DFE Tap-1 Bias Step +1 000000_B: DFE Tap-1 Bias Step +0 (Default)	1,2,3
Sign Bit DQL4 DFE Tap-1 Bias	R/W	OP[6]	0_B: Positive DFE Tap-1 Bias (Default) 1_B: Negative DFE Tap-1 Bias	
Enable/Disable DQL4 DFE Tap-1	R/W	OP[7]	0_B: DFE Tap-1 Disable (Default) 1_B: DFE Tap-1 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.98 MR162 (MA[7:0]=$A2_H$) - DQL4 DFE Tap-2 - Q3'17 Ballot #1845.62

MR162 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQL4 DFE Tap-2 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL4 DFE Tap-2 Bias	R/W	OP[5:0]	111111_B: RFU : 010000_B: RFU 001111_B: DFE Tap-2 Bias Step +15 001110_B: DFE Tap-2 Bias Step +14 001011_B: DFE Tap-2 Bias Step +13 : 000101_B: DFE Tap-2 Bias Step +5 000100_B: DFE Tap-2 Bias Step +4 000011_B: DFE Tap-2 Bias Step +3 000010_B: DFE Tap-2 Bias Step +2 000001_B: DFE Tap-2 Bias Step +1 000000_B: DFE Tap-2 Bias Step +0 (Default)	1,2,3
Sign Bit DQL4 DFE Tap-2 Bias	R/W	OP[6]	0_B: Positive DFE Tap-2 Bias (Default) 1_B: Negative DFE Tap-2 Bias	
Enable/Disable DQL4 DFE Tap-2	R/W	OP[7]	0_B: DFE Tap-2 Disable (Default) 1_B: DFE Tap-2 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.99 MR163 (MA[7:0]=$A3_H$) - DQL4 DFE Tap-3 - Q3'17 Ballot #1845.62

MR163 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQL4 DFE Tap-3 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL4 DFE Tap-3 Bias	R/W	OP[5:0]	111111_B: RFU : 001011_B: RFU 001010_B: DFE Tap-3 Bias Step +12 001011_B: DFE Tap-3 Bias Step +11 001010_B: DFE Tap-3 Bias Step +10 : 000101_B: DFE Tap-3 Bias Step +5 000100_B: DFE Tap-3 Bias Step +4 000011_B: DFE Tap-3 Bias Step +3 000010_B: DFE Tap-3 Bias Step +2 000001_B: DFE Tap-3 Bias Step +1 000000_B: DFE Tap-3 Bias Step +0 (Default)	1,2,3
Sign Bit DQL4 DFE Tap-3 Bias	R/W	OP[6]	0_B: Positive DFE Tap-3 Bias (Default) 1_B: Negative DFE Tap-3 Bias	
Enable/Disable DQL4 DFE Tap-3	R/W	OP[7]	0_B: DFE Tap-3 Disable (Default) 1_B: DFE Tap-3 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.100 MR164 (MA[7:0]=$A4_H$) - DQL4 DFE Tap-4 - Q3'17 Ballot #1845.62

MR164 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQL4 DFE Tap-4 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL4 DFE Tap-4 Bias	R/W	OP[5:0]	111111_B: RFU : 001001_B: RFU 001000_B: DFE Tap-4 Bias Step +8 000111_B: DFE Tap-4 Bias Step +7 000110_B: DFE Tap-4 Bias Step +6 000101_B: DFE Tap-4 Bias Step +5 000100_B: DFE Tap-4 Bias Step +4 000011_B: DFE Tap-4 Bias Step +3 000010_B: DFE Tap-4 Bias Step +2 000001_B: DFE Tap-4 Bias Step +1 000000_B: DFE Tap-4 Bias Step +0 (Default)	1,2,3
Sign Bit DQL4 DFE Tap-4 Bias	R/W	OP[6]	0_B: Positive DFE Tap-4 Bias (Default) 1_B: Negative DFE Tap-4 Bias	
Enable/Disable DQL4 DFE Tap-4	R/W	OP[7]	0_B: DFE Tap-4 Disable (Default) 1_B: DFE Tap-4 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.101 MR165 through MR167 are undefined.

There a currently no plans to utilize these addresses.

3.5.102 MR168 (MA[7:0]=$A8_H$) - DQL5 DFE VGA - Q3'17 Ballot #1845.62

MR168 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	RFU	RFU	Sign Bit	DQL5 DFE Gain Bias		

Function	Register Type	Operand	Data	Notes
DQL5 DFE Gain Bias	R/W	OP[2:0]	111_B: RFU 101_B: RFU 100_B: RFU 011_B: DFE Gain Bias Step +3 010_B: DFE Gain Bias Step +2 001_B: DFE Gain Bias Step +1 000_B: DFE Gain Bias Step +0 (Default)	1,2,3
Sign Bit DQL5 Gain Bias	R/W	OP[3]	0_B: Positive DFE Gain Bias (Default) 1_B: Negative DFE Gain Bias	
RFU	R/W	OP[7:4]	RFU	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.103 MR169 (MA[7:0]=$A9_H$) - DQL5 DFE Tap-1- Q3'17 Ballot #1845.62

MR169 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	RFU	DQL5 DFE Tap-1 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL5 DFE Tap-1 Bias	R/W	OP[5:0]	111111_B: RFU : 101001_B: RFU 101000_B: DFE Tap-1 Bias Step +40 100110_B: DFE Tap-1 Bias Step +39 100101_B: DFE Tap-1 Bias Step +38 : 000101_B: DFE Tap-1 Bias Step +5 000100_B: DFE Tap-1 Bias Step +4 000011_B: DFE Tap-1 Bias Step +3 000010_B: DFE Tap-1 Bias Step +2 000001_B: DFE Tap-1 Bias Step +1 000000_B: DFE Tap-1 Bias Step +0 (Default)	1,2.3
Sign Bit DQL5 DFE Tap-1 Bias	R/W	OP[6]	0_B: Positive DFE Tap-1 Bias (Default) 1_B: Negative DFE Tap-1 Bias	
Enable/Disable DQL5 DFE Tap-1	R/W	OP[7]	0_B: DFE Tap-1 Disable (Default) 1_B: DFE Tap-1 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.104 MR170 (MA[7:0]=AA_H) - DQL5 DFE Tap-2 - Q3'17 Ballot #1845.62

MR170 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQL5 DFE Tap-2 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL5 DFE Tap-2 Bias	R/W	OP[5:0]	111111_B: RFU : 010000_B: RFU 001111_B: DFE Tap-2 Bias Step +15 001110_B: DFE Tap-2 Bias Step +14 001011_B: DFE Tap-2 Bias Step +13 : 000101_B: DFE Tap-2 Bias Step +5 000100_B: DFE Tap-2 Bias Step +4 000011_B: DFE Tap-2 Bias Step +3 000010_B: DFE Tap-2 Bias Step +2 000001_B: DFE Tap-2 Bias Step +1 000000_B: DFE Tap-2 Bias Step +0 (Default)	1,2,3
Sign Bit DQL5 DFE Tap-2 Bias	R/W	OP[6]	0_B: Positive DFE Tap-2 Bias (Default) 1_B: Negative DFE Tap-2 Bias	
Enable/Disable DQL5 DFE Tap-2	R/W	OP[7]	0_B: DFE Tap-2 Disable (Default) 1_B: DFE Tap-2 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.105 MR171 (MA[7:0]=AB_H) - DQL5 DFE Tap-3 - Q3'17 Ballot #1845.62

MR171 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQL5 DFE Tap-3 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL5 DFE Tap-3 Bias	R/W	OP[5:0]	111111_B: RFU : 001011_B: RFU 001010_B: DFE Tap-3 Bias Step +12 001011_B: DFE Tap-3 Bias Step +11 001010_B: DFE Tap-3 Bias Step +10 : 000101_B: DFE Tap-3 Bias Step +5 000100_B: DFE Tap-3 Bias Step +4 000011_B: DFE Tap-3 Bias Step +3 000010_B: DFE Tap-3 Bias Step +2 000001_B: DFE Tap-3 Bias Step +1 000000_B: DFE Tap-3 Bias Step +0 (Default)	1,2,3
Sign Bit DQL5 DFE Tap-3 Bias	R/W	OP[6]	0_B: Positive DFE Tap-3 Bias (Default) 1_B: Negative DFE Tap-3 Bias	
Enable/Disable DQL5 DFE Tap-3	R/W	OP[7]	0_B: DFE Tap-3 Disable (Default) 1_B: DFE Tap-3 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.106 MR172 (MA[7:0]=AC_H) - DQL5 DFE Tap-4 - Q3'17 Ballot #1845.62

MR172 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQL5 DFE Tap-4 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL5 DFE Tap-4 Bias	R/W	OP[5:0]	111111_B: RFU : 001001_B: RFU 001000_B: DFE Tap-4 Bias Step +8 000111_B: DFE Tap-4 Bias Step +7 000110_B: DFE Tap-4 Bias Step +6 000101_B: DFE Tap-4 Bias Step +5 000100_B: DFE Tap-4 Bias Step +4 000011_B: DFE Tap-4 Bias Step +3 000010_B: DFE Tap-4 Bias Step +2 000001_B: DFE Tap-4 Bias Step +1 000000_B: DFE Tap-4 Bias Step +0 (Default)	1,2,3
Sign Bit DQL5 DFE Tap-4 Bias	R/W	OP[6]	0_B: Positive DFE Tap-4 Bias (Default) 1_B: Negative DFE Tap-4 Bias	
Enable/Disable DQL5 DFE Tap-4	R/W	OP[7]	0_B: DFE Tap-4 Disable (Default) 1_B: DFE Tap-4 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.107 MR173 through MR175 are undefined.

There a currently no plans to utilize these addresses.

3.5.108 MR176 (MA[7:0]=$B0_H$) - DQL6 DFE VGA - Q3'17 Ballot #1845.62

MR176 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	RFU	RFU	Sign Bit	DQL6 DFE Gain Bias		

Function	Register Type	Operand	Data	Notes
DQL6 DFE Gain Bias	R/W	OP[2:0]	111B: RFU 101B: RFU 100B: RFU 011B: DFE Gain Bias Step +3 010B: DFE Gain Bias Step +2 001B: DFE Gain Bias Step +1 000B: DFE Gain Bias Step +0 (Default)	1,2,3
Sign Bit DQL6 DFE Gain Bias	R/W	OP[3]	0B: Positive DFE Gain Bias (Default) 1B: Negative DFE Gain Bias	
RFU	R/W	OP[7:4]	RFU	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.109 MR177 (MA[7:0]=$B1_H$) - DQL6 DFE Tap-1- Q3'17 Ballot #1845.62

MR177 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	RFU	DQL6 DFE Tap-1 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL6 DFE Tap-1 Bias	R/W	OP[5:0]	111111_B: RFU : 101001_B: RFU 101000_B: DFE Tap-1 Bias Step +40 100110_B: DFE Tap-1 Bias Step +39 100101_B: DFE Tap-1 Bias Step +38 : 000101_B: DFE Tap-1 Bias Step +5 000100_B: DFE Tap-1 Bias Step +4 000011_B: DFE Tap-1 Bias Step +3 000010_B: DFE Tap-1 Bias Step +2 000001_B: DFE Tap-1 Bias Step +1 000000_B: DFE Tap-1 Bias Step +0 (Default)	1,2,3
Sign Bit DQL6 DFE Tap-1 Bias	R/W	OP[6]	0_B: Positive DFE Tap-1 Bias (Default) 1_B: Negative DFE Tap-1 Bias	
Enable/Disable DQL6 DFE Tap-1	R/W	OP[7]	0_B: DFE Tap-1 Disable (Default) 1_B: DFE Tap-1 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.110 MR178 (MA[7:0]=$B2_H$) - DQL6 DFE Tap-2 - Q3'17 Ballot #1845.62

MR178 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQL6 DFE Tap-2 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL6 DFE Tap-2 Bias	R/W	OP[5:0]	111111_B: RFU : 010000_B: RFU 001111_B: DFE Tap-2 Bias Step +15 001110_B: DFE Tap-2 Bias Step +14 001011_B: DFE Tap-2 Bias Step +13 : 000101_B: DFE Tap-2 Bias Step +5 000100_B: DFE Tap-2 Bias Step +4 000011_B: DFE Tap-2 Bias Step +3 000010_B: DFE Tap-2 Bias Step +2 000001_B: DFE Tap-2 Bias Step +1 000000_B: DFE Tap-2 Bias Step +0 (Default)	1,2,3
Sign Bit DQL6 DFE Tap-2 Bias	R/W	OP[6]	0_B: Positive DFE Tap-2 Bias (Default) 1_B: Negative DFE Tap-2 Bias	
Enable/Disable DQL6 DFE Tap-2	R/W	OP[7]	0_B: DFE Tap-2 Disable (Default) 1_B: DFE Tap-2 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.111 MR179 (MA[7:0]=$B3_H$) - DQL6 DFE Tap-3 - Q3'17 Ballot #1845.62

MR179 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQL6 DFE Tap-3 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL6 DFE Tap-3 Bias	R/W	OP[5:0]	111111_B: RFU : 001011_B: RFU 001010_B: DFE Tap-3 Bias Step +12 001011_B: DFE Tap-3 Bias Step +11 001010_B: DFE Tap-3 Bias Step +10 : 000101_B: DFE Tap-3 Bias Step +5 000100_B: DFE Tap-3 Bias Step +4 000011_B: DFE Tap-3 Bias Step +3 000010_B: DFE Tap-3 Bias Step +2 000001_B: DFE Tap-3 Bias Step +1 000000_B: DFE Tap-3 Bias Step +0 (Default)	1,2,3
Sign Bit DQL6 DFE Tap-3 Bias	R/W	OP[6]	0_B: Positive DFE Tap-3 Bias (Default) 1_B: Negative DFE Tap-3 Bias	
Enable/Disable DQL6 DFE Tap-3	R/W	OP[7]	0_B: DFE Tap-3 Disable (Default) 1_B: DFE Tap-3 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.112 MR180 (MA[7:0]=$B4_H$) - DQL6 DFE Tap-4 - Q3'17 Ballot #1845.62

MR180 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQL6 DFE Tap-4 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL6 DFE Tap-4 Bias	R/W	OP[5:0]	111111_B: RFU : 001001_B: RFU 001000_B: DFE Tap-4 Bias Step +8 000111_B: DFE Tap-4 Bias Step +7 000110_B: DFE Tap-4 Bias Step +6 000101_B: DFE Tap-4 Bias Step +5 000100_B: DFE Tap-4 Bias Step +4 000011_B: DFE Tap-4 Bias Step +3 000010_B: DFE Tap-4 Bias Step +2 000001_B: DFE Tap-4 Bias Step +1 000000_B: DFE Tap-4 Bias Step +0 (Default)	1,2,3
Sign Bit DQL6 DFE Tap-4 Bias	R/W	OP[6]	0_B: Positive DFE Tap-4 Bias (Default) 1_B: Negative DFE Tap-4 Bias	
Enable/Disable DQL6 DFE Tap-4	R/W	OP[7]	0_B: DFE Tap-4 Disable (Default) 1_B: DFE Tap-4 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.113 MR181 through MR183 are undefined.

There a currently no plans to utilize these addresses.

3.5.114 MR184 (MA[7:0]=$B8_H$) - DQL7 DFE VGA - Q3'17 Ballot #1845.62

MR184 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	RFU	RFU	Sign Bit	DQL7 DFE Gain Bias		

Function	Register Type	Operand	Data	Notes
DQL7 DFE Gain Bias	R/W	OP[2:0]	111_B: RFU 101_B: RFU 100_B: RFU 011_B: DFE Gain Bias Step +3 010_B: DFE Gain Bias Step +2 001_B: DFE Gain Bias Step +1 000_B: DFE Gain Bias Step +0 (Default)	1,2,3
Sign Bit DQL7 Gain Bias	R/W	OP[3]	0_B: Positive DFE Gain Bias (Default) 1_B: Negative DFE Gain Bias	
RFU	R/W	OP[7:4]	RFU	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.115 MR185 (MA[7:0]=$B9_H$) - DQL7 DFE Tap-1 - Q3'17 Ballot #1845.62

MR185 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	RFU	DQL7 DFE Tap-1 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL7 DFE Tap-1 Bias	R/W	OP[5:0]	111111_B: RFU : 101001_B: RFU 101000_B: DFE Tap-1 Bias Step +40 100110_B: DFE Tap-1 Bias Step +39 100101_B: DFE Tap-1 Bias Step +38 : 000101_B: DFE Tap-1 Bias Step +5 000100_B: DFE Tap-1 Bias Step +4 000011_B: DFE Tap-1 Bias Step +3 000010_B: DFE Tap-1 Bias Step +2 000001_B: DFE Tap-1 Bias Step +1 000000_B: DFE Tap-1 Bias Step +0 (Default)	1,2,3
Sign Bit DQL7 DFE Tap-1 Bias	R/W	OP[6]	0_B: Positive DFE Tap-1 Bias (Default) 1_B: Negative DFE Tap-1 Bias	
Enable/Disable DQL7 DFE Tap-1	R/W	OP[7]	0_B: DFE Tap-1 Disable (Default) 1_B: DFE Tap-1 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.116 MR186 (MA[7:0]=BA_H) - DQL7 DFE Tap-2 - Q3'17 Ballot #1845.62

MR186 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQL7 DFE Tap-2 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL7 DFE Tap-2 Bias	R/W	OP[5:0]	111111_B: RFU : 010000_B: RFU 001111_B: DFE Tap-2 Bias Step +15 001110_B: DFE Tap-2 Bias Step +14 001011_B: DFE Tap-2 Bias Step +13 : 000101_B: DFE Tap-2 Bias Step +5 000100_B: DFE Tap-2 Bias Step +4 000011_B: DFE Tap-2 Bias Step +3 000010_B: DFE Tap-2 Bias Step +2 000001_B: DFE Tap-2 Bias Step +1 000000_B: DFE Tap-2 Bias Step +0 (Default)	1,2,3
Sign Bit DQL7 DFE Tap-2 Bias	R/W	OP[6]	0_B: Positive DFE Tap-2 Bias (Default) 1_B: Negative DFE Tap-2 Bias	
Enable/Disable DQL7 DFE Tap-2	R/W	OP[7]	0_B: DFE Tap-2 Disable (Default) 1_B: DFE Tap-2 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.117 MR187 (MA[7:0]=BB_H) - DQL7 DFE Tap-3 - Q3'17 Ballot #1845.62

MR187 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQL7 DFE Tap-3 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL7 DFE Tap-3 Bias	R/W	OP[5:0]	111111_B: RFU : 001011_B: RFU 001010_B: DFE Tap-3 Bias Step +12 001011_B: DFE Tap-3 Bias Step +11 001010_B: DFE Tap-3 Bias Step +10 : 000101_B: DFE Tap-3 Bias Step +5 000100_B: DFE Tap-3 Bias Step +4 000011_B: DFE Tap-3 Bias Step +3 000010_B: DFE Tap-3 Bias Step +2 000001_B: DFE Tap-3 Bias Step +1 000000_B: DFE Tap-3 Bias Step +0 (Default)	1,2,3
Sign Bit DQL7 DFE Tap-3 Bias	R/W	OP[6]	0_B: Positive DFE Tap-3 Bias (Default) 1_B: Negative DFE Tap-3 Bias	
Enable/Disable DQL7 DFE Tap-3	R/W	OP[7]	0_B: DFE Tap-3 Disable (Default) 1_B: DFE Tap-3 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.118 MR188 (MA[7:0]=BC_H) - DQL7 DFE Tap-4 - Q3'17 Ballot #1845.62

MR188 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQL7 DFE Tap-4 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQL7 DFE Tap-4 Bias	R/W	OP[5:0]	111111_B: RFU : 001001_B: RFU 001000_B: DFE Tap-4 Bias Step +8 000111_B: DFE Tap-4 Bias Step +7 000110_B: DFE Tap-4 Bias Step +6 000101_B: DFE Tap-4 Bias Step +5 000100_B: DFE Tap-4 Bias Step +4 000011_B: DFE Tap-4 Bias Step +3 000010_B: DFE Tap-4 Bias Step +2 000001_B: DFE Tap-4 Bias Step +1 000000_B: DFE Tap-4 Bias Step +0 (Default)	1,2,3
Sign Bit DQL7 DFE Tap-4 Bias	R/W	OP[6]	0_B: Positive DFE Tap-4 Bias (Default) 1_B: Negative DFE Tap-4 Bias	
Enable/Disable DQL7 DFE Tap-4	R/W	OP[7]	0_B: DFE Tap-4 Disable (Default) 1_B: DFE Tap-4 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.119 MR189 through MR191 are undefined.

There a currently no plans to utilize these addresses.

3.5.120 MR192 (MA[7:0]=$C0_H$) - DQLU0 DFE VGA - Q3'17 Ballot #1845.62

MR192 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	RFU	RFU	Sign Bit	DQU0 DFE Gain Bias		

Function	Register Type	Operand	Data	Notes
DQU0 DFE Gain Bias	R/W	OP[2:0]	111_B: RFU 101_B: RFU 100_B: RFU 011_B: DFE Gain Bias Step +3 010_B: DFE Gain Bias Step +2 001_B: DFE Gain Bias Step +1 000_B: DFE Gain Bias Step +0 (Default)	1,2,3
Sign Bit DQU0 DFE Gain Bias	R/W	OP[3]	0_B: Positive DFE Gain Bias (Default) 1_B: Negative DFE Gain Bias	
RFU	R/W	OP[7:4]	RFU	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.121 MR193 (MA[7:0]=$C1_H$) - DQU0 DFE Tap-1 - Q3'17 Ballot #1845.62

MR193 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	RFU	DQU0 DFE Tap-1 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU0 DFE Tap-1 Bias	R/W	OP[5:0]	111111_B: RFU : 101001_B: RFU 101000_B: DFE Tap-1 Bias Step +40 100110_B: DFE Tap-1 Bias Step +39 100101_B: DFE Tap-1 Bias Step +38 : 000101_B: DFE Tap-1 Bias Step +5 000100_B: DFE Tap-1 Bias Step +4 000011_B: DFE Tap-1 Bias Step +3 000010_B: DFE Tap-1 Bias Step +2 000001_B: DFE Tap-1 Bias Step +1 000000_B: DFE Tap-1 Bias Step +0 (Default)	1,2,3
Sign Bit DQU0 DFE Tap-1 Bias	R/W	OP[6]	0_B: Positive DFE Tap-1 Bias (Default) 1_B: Negative DFE Tap-1 Bias	
Enable/Disable DQU0 DFE Tap-1	R/W	OP[7]	0_B: DFE Tap-1 Disable (Default) 1_B: DFE Tap-1 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.122 MR194 (MA[7:0]=$C2_H$) - DQU0 DFE Tap-2 - Q3'17 Ballot #1845.62

MR194 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQU0 DFE Tap-2 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU0 DFE Tap-2 Bias	R/W	OP[5:0]	111111_B: RFU : 010000_B: RFU 001111_B: DFE Tap-2 Bias Step +15 001110_B: DFE Tap-2 Bias Step +14 001011_B: DFE Tap-2 Bias Step +13 : 000101_B: DFE Tap-2 Bias Step +5 000100_B: DFE Tap-2 Bias Step +4 000011_B: DFE Tap-2 Bias Step +3 000010_B: DFE Tap-2 Bias Step +2 000001_B: DFE Tap-2 Bias Step +1 000000_B: DFE Tap-2 Bias Step +0 (Default)	1,2,3
Sign Bit DQU0 DFE Tap-2 Bias	R/W	OP[6]	0_B: Positive DFE Tap-2 Bias (Default) 1_B: Negative DFE Tap-2 Bias	
Enable/Disable DQU0 DFE Tap-2	R/W	OP[7]	0_B: DFE Tap-2 Disable (Default) 1_B: DFE Tap-2 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.123 MR195 (MA[7:0]=$C3_H$) - DQU0 DFE Tap-3 - Q3'17 Ballot #1845.62

MR195 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQU0 DFE Tap-3 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU0 DFE Tap-3 Bias	R/W	OP[5:0]	111111_B: RFU : 001011_B: RFU 001010_B: DFE Tap-3 Bias Step +12 001011_B: DFE Tap-3 Bias Step +11 001010_B: DFE Tap-3 Bias Step +10 : 000101_B: DFE Tap-3 Bias Step +5 000100_B: DFE Tap-3 Bias Step +4 000011_B: DFE Tap-3 Bias Step +3 000010_B: DFE Tap-3 Bias Step +2 000001_B: DFE Tap-3 Bias Step +1 000000_B: DFE Tap-3 Bias Step +0 (Default)	1,2,3
Sign Bit DQU0 DFE Tap-3 Bias	R/W	OP[6]	0_B: Positive DFE Tap-3 Bias (Default) 1_B: Negative DFE Tap-3 Bias	
Enable/Disable DQU0 DFE Tap-3	R/W	OP[7]	0_B: DFE Tap-3 Disable (Default) 1_B: DFE Tap-3 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.124 MR196 (MA[7:0]=$C4_H$) - DQU0 DFE Tap-4 - Q3'17 Ballot #1845.62

MR196 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQU0 DFE Tap-4 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU0 DFE Tap-4 Bias	R/W	OP[5:0]	111111_B: RFU : 001001_B: RFU 001000_B: DFE Tap-4 Bias Step +8 000111_B: DFE Tap-4 Bias Step +7 000110_B: DFE Tap-4 Bias Step +6 000101_B: DFE Tap-4 Bias Step +5 000100_B: DFE Tap-4 Bias Step +4 000011_B: DFE Tap-4 Bias Step +3 000010_B: DFE Tap-4 Bias Step +2 000001_B: DFE Tap-4 Bias Step +1 000000_B: DFE Tap-4 Bias Step +0 (Default)	1,2,3
Sign Bit DQU0 DFE Tap-4 Bias	R/W	OP[6]	0_B: Positive DFE Tap-4 Bias (Default) 1_B: Negative DFE Tap-4 Bias	
Enable/Disable DQU0 DFE Tap-4	R/W	OP[7]	0_B: DFE Tap-4 Disable (Default) 1_B: DFE Tap-4 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.125 MR197 through MR199 are undefined.

There a currently no plans to utilize these addresses.

3.5.126 MR200 (MA[7:0]=$C8_H$) - DQU1 DFE VGA - Q3'17 Ballot #1845.62

MR200 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	RFU	RFU	Sign Bit	DQU1 DFE Gain Bias		

Function	Register Type	Operand	Data	Notes
DQU1 DFE Gain Bias	R/W	OP[2:0]	111_B: RFU 101_B: RFU 100_B: RFU 011_B: DFE Gain Bias Step +3 010_B: DFE Gain Bias Step +2 001_B: DFE Gain Bias Step +1 000_B: DFE Gain Bias Step +0 (Default)	1,2,3
Sign Bit DQU1 Gain Bias	R/W	OP[3]	0_B: Positive DFE Gain Bias (Default) 1_B: Negative DFE Gain Bias	
RFU	R/W	OP[7:4]	RFU	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.127 MR201 (MA[7:0]=$C9_H$) - DQU1 DFE Tap-1 - Q3'17 Ballot #1845.62

MR201 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	RFU	DQU1 DFE Tap-1 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU1 DFE Tap-1 Bias	R/W	OP[5:0]	111111_B: RFU : 101001_B: RFU 101000_B: DFE Tap-1 Bias Step +40 100110_B: DFE Tap-1 Bias Step +39 100101_B: DFE Tap-1 Bias Step +38 : 000101_B: DFE Tap-1 Bias Step +5 000100_B: DFE Tap-1 Bias Step +4 000011_B: DFE Tap-1 Bias Step +3 000010_B: DFE Tap-1 Bias Step +2 000001_B: DFE Tap-1 Bias Step +1 000000_B: DFE Tap-1 Bias Step +0 (Default)	1,2,3
Sign Bit DQU1 DFE Tap-1 Bias	R/W	OP[6]	0_B: Positive DFE Tap-1 Bias (Default) 1_B: Negative DFE Tap-1 Bias	
Enable/Disable DQU1 DFE Tap-1	R/W	OP[7]	0_B: DFE Tap-1 Disable (Default) 1_B: DFE Tap-1 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.128 MR202 (MA[7:0]=CA_H) - DQU1 DFE Tap-2 - Q3'17 Ballot #1845.62

MR202 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQU1 DFE Tap-2 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU1 DFE Tap-2 Bias	R/W	OP[5:0]	111111_B: RFU : 010000_B: RFU 001111_B: DFE Tap-2 Bias Step +15 001110_B: DFE Tap-2 Bias Step +14 001011_B: DFE Tap-2 Bias Step +13 : 000101_B: DFE Tap-2 Bias Step +5 000100_B: DFE Tap-2 Bias Step +4 000011_B: DFE Tap-2 Bias Step +3 000010_B: DFE Tap-2 Bias Step +2 000001_B: DFE Tap-2 Bias Step +1 000000_B: DFE Tap-2 Bias Step +0 (Default)	1,2,3
Sign Bit DQU1 DFE Tap-2 Bias	R/W	OP[6]	0_B: Positive DFE Tap-2 Bias (Default) 1_B: Negative DFE Tap-2 Bias	
Enable/Disable DQU1 DFE Tap-2	R/W	OP[7]	0_B: DFE Tap-2 Disable (Default) 1_B: DFE Tap-2 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.129 MR203 (MA[7:0]=CB_H) - DQU1 DFE Tap-3 - Q3'17 Ballot #1845.62

MR203 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQU1 DFE Tap-3 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU1 DFE Tap-3 Bias	R/W	OP[5:0]	111111_B: RFU : 001011_B: RFU 001010_B: DFE Tap-3 Bias Step +12 001011_B: DFE Tap-3 Bias Step +11 001010_B: DFE Tap-3 Bias Step +10 : 000101_B: DFE Tap-3 Bias Step +5 000100_B: DFE Tap-3 Bias Step +4 000011_B: DFE Tap-3 Bias Step +3 000010_B: DFE Tap-3 Bias Step +2 000001_B: DFE Tap-3 Bias Step +1 000000_B: DFE Tap-3 Bias Step +0 (Default)	1,2,3
Sign Bit DQU1 DFE Tap-3 Bias	R/W	OP[6]	0_B: Positive DFE Tap-3 Bias (Default) 1_B: Negative DFE Tap-3 Bias	
Enable/Disable DQU1 DFE Tap-3	R/W	OP[7]	0_B: DFE Tap-3 Disable (Default) 1_B: DFE Tap-3 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.130 MR204 (MA[7:0]=CC_H) - DQU1 DFE Tap-4 - Q3'17 Ballot #1845.62

MR204 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQU1 DFE Tap-4 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU1 DFE Tap-4 Bias	R/W	OP[5:0]	111111_B: RFU : 001001_B: RFU 001000_B: DFE Tap-4 Bias Step +8 000111_B: DFE Tap-4 Bias Step +7 000110_B: DFE Tap-4 Bias Step +6 000101_B: DFE Tap-4 Bias Step +5 000100_B: DFE Tap-4 Bias Step +4 000011_B: DFE Tap-4 Bias Step +3 000010_B: DFE Tap-4 Bias Step +2 000001_B: DFE Tap-4 Bias Step +1 000000_B: DFE Tap-4 Bias Step +0 (Default)	1,2,3
Sign Bit DQU1 DFE Tap-4 Bias	R/W	OP[6]	0_B: Positive DFE Tap-4 Bias (Default) 1_B: Negative DFE Tap-4 Bias	
Enable/Disable DQU1 DFE Tap-4	R/W	OP[7]	0_B: DFE Tap-4 Disable (Default) 1_B: DFE Tap-4 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.131 MR205 through MR207 are undefined.

There a currently no plans to utilize these addresses.

3.5.132 MR208 (MA[7:0]=$D0_H$) - DQU2 DFE VGA - Q3'17 Ballot #1845.62

MR208 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	RFU	RFU	Sign Bit	DQU2 DFE Gain Bias		

Function	Register Type	Operand	Data	Notes
DQU2 DFE Gain Bias	R/W	OP[2:0]	111_B: RFU 101_B: RFU 100_B: RFU 011_B: DFE Gain Bias Step +3 010_B: DFE Gain Bias Step +2 001_B: DFE Gain Bias Step +1 000_B: DFE Gain Bias Step +0 (Default)	1,2,3
Sign Bit DQU2 DFE Gain Bias	R/W	OP[3]	0_B: Positive DFE Gain Bias (Default) 1_B: Negative DFE Gain Bias	
RFU	R/W	OP[7:4]	RFU	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.133 MR209 (MA[7:0]=$D1_H$) - DQU2 DFE Tap-1 - Q3'17 Ballot #1845.62

MR209 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	RFU	DQU2 DFE Tap-1 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU2 DFE Tap-1 Bias	R/W	OP[5:0]	111111_B: RFU : 101001_B: RFU 101000_B: DFE Tap-1 Bias Step +40 100110_B: DFE Tap-1 Bias Step +39 100101_B: DFE Tap-1 Bias Step +38 : 000101_B: DFE Tap-1 Bias Step +5 000100_B: DFE Tap-1 Bias Step +4 000011_B: DFE Tap-1 Bias Step +3 000010_B: DFE Tap-1 Bias Step +2 000001_B: DFE Tap-1 Bias Step +1 000000_B: DFE Tap-1 Bias Step +0 (Default)	1,2,3
Sign Bit DQU2 DFE Tap-1 Bias	R/W	OP[6]	0_B: Positive DFE Tap-1 Bias (Default) 1_B: Negative DFE Tap-1 Bias	
Enable/Disable DQU2 DFE Tap-1	R/W	OP[7]	0_B: DFE Tap-1 Disable (Default) 1_B: DFE Tap-1 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.134 MR210 (MA[7:0]=$D2_H$) - DQU2 DFE Tap-2 - Q3'17 Ballot #1845.62

MR210 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQU2 DFE Tap-2 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU2 DFE Tap-2 Bias	R/W	OP[5:0]	111111_B: RFU : 010000_B: RFU 001111_B: DFE Tap-2 Bias Step +15 001110_B: DFE Tap-2 Bias Step +14 001011_B: DFE Tap-2 Bias Step +13 : 000101_B: DFE Tap-2 Bias Step +5 000100_B: DFE Tap-2 Bias Step +4 000011_B: DFE Tap-2 Bias Step +3 000010_B: DFE Tap-2 Bias Step +2 000001_B: DFE Tap-2 Bias Step +1 000000_B: DFE Tap-2 Bias Step +0 (Default)	1,2,3
Sign Bit DQU2 DFE Tap-2 Bias	R/W	OP[6]	0_B: Positive DFE Tap-2 Bias (Default) 1_B: Negative DFE Tap-2 Bias	
Enable/Disable DQU2 DFE Tap-2	R/W	OP[7]	0_B: DFE Tap-2 Disable (Default) 1_B: DFE Tap-2 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.135 MR211 (MA[7:0]=$D3_H$) - DQU2 DFE Tap-3 - Q3'17 Ballot #1845.62

MR211 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQU2 DFE Tap-3 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU2 DFE Tap-3 Bias	R/W	OP[5:0]	111111_B: RFU : 001011_B: RFU 001010_B: DFE Tap-3 Bias Step +12 001011_B: DFE Tap-3 Bias Step +11 001010_B: DFE Tap-3 Bias Step +10 : 000101_B: DFE Tap-3 Bias Step +5 000100_B: DFE Tap-3 Bias Step +4 000011_B: DFE Tap-3 Bias Step +3 000010_B: DFE Tap-3 Bias Step +2 000001_B: DFE Tap-3 Bias Step +1 000000_B: DFE Tap-3 Bias Step +0 (Default)	1,2,3
Sign Bit DQU2 DFE Tap-3 Bias	R/W	OP[6]	0_B: Positive DFE Tap-3 Bias (Default) 1_B: Negative DFE Tap-3 Bias	
Enable/Disable DQU2 DFE Tap-3	R/W	OP[7]	0_B: DFE Tap-3 Disable (Default) 1_B: DFE Tap-3 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.136 MR212 (MA[7:0]=$D4_H$) - DQU2 DFE Tap-4 - Q3'17 Ballot #1845.62

MR212 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQU2 DFE Tap-4 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU2 DFE Tap-4 Bias	R/W	OP[5:0]	111111_B: RFU : 001001_B: RFU 001000_B: DFE Tap-4 Bias Step +8 000111_B: DFE Tap-4 Bias Step +7 000110_B: DFE Tap-4 Bias Step +6 000101_B: DFE Tap-4 Bias Step +5 000100_B: DFE Tap-4 Bias Step +4 000011_B: DFE Tap-4 Bias Step +3 000010_B: DFE Tap-4 Bias Step +2 000001_B: DFE Tap-4 Bias Step +1 000000_B: DFE Tap-4 Bias Step +0 (Default)	1,2,3
Sign Bit DQU2 DFE Tap-4 Bias	R/W	OP[6]	0_B: Positive DFE Tap-4 Bias (Default) 1_B: Negative DFE Tap-4 Bias	
Enable/Disable DQU2 DFE Tap-4	R/W	OP[7]	0_B: DFE Tap-4 Disable (Default) 1_B: DFE Tap-4 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.137 MR213 through MR215 are undefined.

There a currently no plans to utilize these addresses.

3.5.138 MR216 (MA[7:0]=$D8_H$) - DQU3 DFE VGA - Q3'17 Ballot #1845.62

MR216 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	RFU	RFU	Sign Bit	DQU3 DFE Gain Bias		

Function	Register Type	Operand	Data	Notes
DQU3 DFE Gain Bias	R/W	OP[2:0]	111_B: RFU 101_B: RFU 100_B: RFU 011_B: DFE Gain Bias Step +3 010_B: DFE Gain Bias Step +2 001_B: DFE Gain Bias Step +1 000_B: DFE Gain Bias Step +0 (Default)	1,2,3
Sign Bit DQU3 Gain Bias	R/W	OP[3]	0_B: Positive DFE Gain Bias (Default) 1_B: Negative DFE Gain Bias	
RFU	R/W	OP[7:4]	RFU	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.139 MR217 (MA[7:0]=$D9_H$) - DQU3 DFE Tap-1 - Q3'17 Ballot #1845.62

MR217 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	RFU	DQU3 DFE Tap-1 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU3 DFE Tap-1 Bias	R/W	OP[5:0]	111111_B: RFU : 101001_B: RFU 101000_B: DFE Tap-1 Bias Step +40 100110_B: DFE Tap-1 Bias Step +39 100101_B: DFE Tap-1 Bias Step +38 : 000101_B: DFE Tap-1 Bias Step +5 000100_B: DFE Tap-1 Bias Step +4 000011_B: DFE Tap-1 Bias Step +3 000010_B: DFE Tap-1 Bias Step +2 000001_B: DFE Tap-1 Bias Step +1 000000_B: DFE Tap-1 Bias Step +0 (Default)	1,2,3
Sign Bit DQU3 DFE Tap-1 Bias	R/W	OP[6]	0_B: Positive DFE Tap-1 Bias (Default) 1_B: Negative DFE Tap-1 Bias	
Enable/Disable DQU3 DFE Tap-1	R/W	OP[7]	0_B: DFE Tap-1 Disable (Default) 1_B: DFE Tap-1 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.140 MR218 (MA[7:0]=DA_H) - DQU3 DFE Tap-2 - Q3'17 Ballot #1845.62

MR218 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQU3 DFE Tap-2 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU3 DFE Tap-2 Bias	R/W	OP[5:0]	111111_B: RFU : 010000_B: RFU 001111_B: DFE Tap-2 Bias Step +15 001110_B: DFE Tap-2 Bias Step +14 001011_B: DFE Tap-2 Bias Step +13 : 000101_B: DFE Tap-2 Bias Step +5 000100_B: DFE Tap-2 Bias Step +4 000011_B: DFE Tap-2 Bias Step +3 000010_B: DFE Tap-2 Bias Step +2 000001_B: DFE Tap-2 Bias Step +1 000000_B: DFE Tap-2 Bias Step +0 (Default)	1,2,3
Sign Bit DQU3 DFE Tap-2 Bias	R/W	OP[6]	0_B: Positive DFE Tap-2 Bias (Default) 1_B: Negative DFE Tap-2 Bias	
Enable/Disable DQU3 DFE Tap-2	R/W	OP[7]	0_B: DFE Tap-2 Disable (Default) 1_B: DFE Tap-2 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.141 MR219 (MA[7:0]=DB_H) - DQU3 DFE Tap-3 - Q3'17 Ballot #1845.62

MR219 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQU3 DFE Tap-3 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU3 DFE Tap-3 Bias	R/W	OP[5:0]	111111_B: RFU : 001011_B: RFU 001010_B: DFE Tap-3 Bias Step +12 001011_B: DFE Tap-3 Bias Step +11 001010_B: DFE Tap-3 Bias Step +10 : 000101_B: DFE Tap-3 Bias Step +5 000100_B: DFE Tap-3 Bias Step +4 000011_B: DFE Tap-3 Bias Step +3 000010_B: DFE Tap-3 Bias Step +2 000001_B: DFE Tap-3 Bias Step +1 000000_B: DFE Tap-3 Bias Step +0 (Default)	1,2,3
Sign Bit DQU3 DFE Tap-3 Bias	R/W	OP[6]	0_B: Positive DFE Tap-3 Bias (Default) 1_B: Negative DFE Tap-3 Bias	
Enable/Disable DQU3 DFE Tap-3	R/W	OP[7]	0_B: DFE Tap-3 Disable (Default) 1_B: DFE Tap-3 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.142 MR220 (MA[7:0]=DC_H) - DQU3 DFE Tap-4- Q3'17 Ballot #1845.62

MR220 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQU3 DFE Tap-4 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU3 DFE Tap-4 Bias	R/W	OP[5:0]	111111_B: RFU : 001001_B: RFU 001000_B: DFE Tap-4 Bias Step +8 000111_B: DFE Tap-4 Bias Step +7 000110_B: DFE Tap-4 Bias Step +6 000101_B: DFE Tap-4 Bias Step +5 000100_B: DFE Tap-4 Bias Step +4 000011_B: DFE Tap-4 Bias Step +3 000010_B: DFE Tap-4 Bias Step +2 000001_B: DFE Tap-4 Bias Step +1 000000_B: DFE Tap-4 Bias Step +0 (Default)	1,2,3
Sign Bit DQU3 DFE Tap-4 Bias	R/W	OP[6]	0_B: Positive DFE Tap-4 Bias (Default) 1_B: Negative DFE Tap-4 Bias	
Enable/Disable DQU3 DFE Tap-4	R/W	OP[7]	0_B: DFE Tap-4 Disable (Default) 1_B: DFE Tap-4 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.143 MR221 through MR223 are undefined.

There a currently no plans to utilize these addresses.

3.5.144 MR224 (MA[7:0]=$E0_H$) - DQU4 DFE VGA - Q3'17 Ballot #1845.62

MR224 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	RFU	RFU	Sign Bit	DQU4 DFE Gain Bias		

Function	Register Type	Operand	Data	Notes
DQU4 DFE Gain Bias	R/W	OP[2:0]	111_B: RFU 101_B: RFU 100_B: RFU 011_B: DFE Gain Bias Step +3 010_B: DFE Gain Bias Step +2 001_B: DFE Gain Bias Step +1 000_B: DFE Gain Bias Step +0 (Default)	1,2,3
Sign Bit DQU4 DFE Gain Bias	R/W	OP[3]	0_B: Positive DFE Gain Bias (Default) 1_B: Negative DFE Gain Bias	
RFU	R/W	OP[7:4]	RFU	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.145 MR225 (MA[7:0]=$E1_H$) - DQU4 DFE Tap-1 - Q3'17 Ballot #1845.62

MR225 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	RFU	DQU4 DFE Tap-1 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU4 DFE Tap-1 Bias	R/W	OP[5:0]	111111_B: RFU : 101001_B: RFU 101000_B: DFE Tap-1 Bias Step +40 100110_B: DFE Tap-1 Bias Step +39 100101_B: DFE Tap-1 Bias Step +38 : 000101_B: DFE Tap-1 Bias Step +5 000100_B: DFE Tap-1 Bias Step +4 000011_B: DFE Tap-1 Bias Step +3 000010_B: DFE Tap-1 Bias Step +2 000001_B: DFE Tap-1 Bias Step +1 000000_B: DFE Tap-1 Bias Step +0 (Default)	1,2,3
Sign Bit DQU4 DFE Tap-1 Bias	R/W	OP[6]	0_B: Positive DFE Tap-1 Bias (Default) 1_B: Negative DFE Tap-1 Bias	
Enable/Disable DQU4 DFE Tap-1	R/W	OP[7]	0_B: DFE Tap-1 Disable (Default) 1_B: DFE Tap-1 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.146 MR226 (MA[7:0]=$E2_H$) - DQU4 DFE Tap-2 - Q3'17 Ballot #1845.62

MR226 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQU4 DFE Tap-2 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU4 DFE Tap-2 Bias	R/W	OP[5:0]	111111_B: RFU : 010000_B: RFU 001111_B: DFE Tap-2 Bias Step +15 001110_B: DFE Tap-2 Bias Step +14 001011_B: DFE Tap-2 Bias Step +13 : 000101_B: DFE Tap-2 Bias Step +5 000100_B: DFE Tap-2 Bias Step +4 000011_B: DFE Tap-2 Bias Step +3 000010_B: DFE Tap-2 Bias Step +2 000001_B: DFE Tap-2 Bias Step +1 000000_B: DFE Tap-2 Bias Step +0 (Default)	1,2,3
Sign Bit DQU4 DFE Tap-2 Bias	R/W	OP[6]	0_B: Positive DFE Tap-2 Bias (Default) 1_B: Negative DFE Tap-2 Bias	
Enable/Disable DQU4 DFE Tap-2	R/W	OP[7]	0_B: DFE Tap-2 Disable (Default) 1_B: DFE Tap-2 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.147 MR227 (MA[7:0]=$E3_H$) - DQU4 DFE Tap-3 - Q3'17 Ballot #1845.62

MR227 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQU4 DFE Tap-3 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU4 DFE Tap-3 Bias	R/W	OP[5:0]	111111_B: RFU : 001011_B: RFU 001010_B: DFE Tap-3 Bias Step +12 001011_B: DFE Tap-3 Bias Step +11 001010_B: DFE Tap-3 Bias Step +10 : 000101_B: DFE Tap-3 Bias Step +5 000100_B: DFE Tap-3 Bias Step +4 000011_B: DFE Tap-3 Bias Step +3 000010_B: DFE Tap-3 Bias Step +2 000001_B: DFE Tap-3 Bias Step +1 000000_B: DFE Tap-3 Bias Step +0 (Default)	1,2,3
Sign Bit DQU4 DFE Tap-3 Bias	R/W	OP[6]	0_B: Positive DFE Tap-3 Bias (Default) 1_B: Negative DFE Tap-3 Bias	
Enable/Disable DQU4 DFE Tap-3	R/W	OP[7]	0_B: DFE Tap-3 Disable (Default) 1_B: DFE Tap-3 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.148 MR228 (MA[7:0]=$E4_H$) - DQU4 DFE Tap-4 - Q3'17 Ballot #1845.62

MR228 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQU4 DFE Tap-4 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU4 DFE Tap-4 Bias	R/W	OP[5:0]	111111_B: RFU : 001001_B: RFU 001000_B: DFE Tap-4 Bias Step +8 000111_B: DFE Tap-4 Bias Step +7 000110_B: DFE Tap-4 Bias Step +6 000101_B: DFE Tap-4 Bias Step +5 000100_B: DFE Tap-4 Bias Step +4 000011_B: DFE Tap-4 Bias Step +3 000010_B: DFE Tap-4 Bias Step +2 000001_B: DFE Tap-4 Bias Step +1 000000_B: DFE Tap-4 Bias Step +0 (Default)	1,2,3
Sign Bit DQU4 DFE Tap-4 Bias	R/W	OP[6]	0_B: Positive DFE Tap-4 Bias (Default) 1_B: Negative DFE Tap-4 Bias	
Enable/Disable DQU4 DFE Tap-4	R/W	OP[7]	0_B: DFE Tap-4 Disable (Default) 1_B: DFE Tap-4 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.149 MR229 through MR231 are undefined.

There a currently no plans to utilize these addresses.

3.5.150 MR232 (MA[7:0]=$E8_H$) - DQU5 DFE VGA - Q3'17 Ballot #1845.62

MR232 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	RFU	RFU	Sign Bit	DQU5 DFE Gain Bias		

Function	Register Type	Operand	Data	Notes
DQU5 DFE Gain Bias	R/W	OP[2:0]	111_B: RFU 101_B: RFU 100_B: RFU 011_B: DFE Gain Bias Step +3 010_B: DFE Gain Bias Step +2 001_B: DFE Gain Bias Step +1 000_B: DFE Gain Bias Step +0 (Default)	1,2,3
Sign Bit DQU5 Gain Bias	R/W	OP[3]	0_B: Positive DFE Gain Bias (Default) 1_B: Negative DFE Gain Bias	
RFU	R/W	OP[7:4]	RFU	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.151 MR233 (MA[7:0]=$E9_H$) - DQU5 DFE Tap-1 - Q3'17 Ballot #1845.62

MR233 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	RFU	DQU5 DFE Tap-1 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU5 DFE Tap-1 Bias	R/W	OP[5:0]	111111_B: RFU : 101001_B: RFU 101000_B: DFE Tap-1 Bias Step +40 100110_B: DFE Tap-1 Bias Step +39 100101_B: DFE Tap-1 Bias Step +38 : 000101_B: DFE Tap-1 Bias Step +5 000100_B: DFE Tap-1 Bias Step +4 000011_B: DFE Tap-1 Bias Step +3 000010_B: DFE Tap-1 Bias Step +2 000001_B: DFE Tap-1 Bias Step +1 000000_B: DFE Tap-1 Bias Step +0 (Default)	1,2,3
Sign Bit DQU5 DFE Tap-1 Bias	R/W	OP[6]	0_B: Positive DFE Tap-1 Bias (Default) 1_B: Negative DFE Tap-1 Bias	
Enable/Disable DQU5 DFE Tap-1	R/W	OP[7]	0_B: DFE Tap-1 Disable (Default) 1_B: DFE Tap-1 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.152 MR234 (MA[7:0]=EA_H) - DQU5 DFE Tap-2 - Q3'17 Ballot #1845.62

MR234 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQU5 DFE Tap-2 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU5 DFE Tap-2 Bias	R/W	OP[5:0]	111111_B: RFU : 010000_B: RFU 001111_B: DFE Tap-2 Bias Step +15 001110_B: DFE Tap-2 Bias Step +14 001011_B: DFE Tap-2 Bias Step +13 : 000101_B: DFE Tap-2 Bias Step +5 000100_B: DFE Tap-2 Bias Step +4 000011_B: DFE Tap-2 Bias Step +3 000010_B: DFE Tap-2 Bias Step +2 000001_B: DFE Tap-2 Bias Step +1 000000_B: DFE Tap-2 Bias Step +0 (Default)	1,2,3
Sign Bit DQU5 DFE Tap-2 Bias	R/W	OP[6]	0_B: Positive DFE Tap-2 Bias (Default) 1_B: Negative DFE Tap-2 Bias	
Enable/Disable DQU5 DFE Tap-2	R/W	OP[7]	0_B: DFE Tap-2 Disable (Default) 1_B: DFE Tap-2 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.153 MR235 (MA[7:0]=EB_H) - DQU5 DFE Tap-3 - Q3'17 Ballot #1845.62

MR235 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQU5 DFE Tap-3 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU5 DFE Tap-3 Bias	R/W	OP[5:0]	111111_B: RFU : 001011_B: RFU 001010_B: DFE Tap-3 Bias Step +12 001011_B: DFE Tap-3 Bias Step +11 001010_B: DFE Tap-3 Bias Step +10 : 000101_B: DFE Tap-3 Bias Step +5 000100_B: DFE Tap-3 Bias Step +4 000011_B: DFE Tap-3 Bias Step +3 000010_B: DFE Tap-3 Bias Step +2 000001_B: DFE Tap-3 Bias Step +1 000000_B: DFE Tap-3 Bias Step +0 (Default)	1,2,3
Sign Bit DQU5 DFE Tap-3 Bias	R/W	OP[6]	0_B: Positive DFE Tap-3 Bias (Default) 1_B: Negative DFE Tap-3 Bias	
Enable/Disable DQU5 DFE Tap-3	R/W	OP[7]	0_B: DFE Tap-3 Disable (Default) 1_B: DFE Tap-3 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.154 MR236 (MA[7:0]=EC_H) - DQU5 DFE Tap-4 - Q3'17 Ballot #1845.62

MR236 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQU5 DFE Tap-4 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU5 DFE Tap-4 Bias	R/W	OP[5:0]	111111_B: RFU : 001001_B: RFU 001000_B: DFE Tap-4 Bias Step +8 000111_B: DFE Tap-4 Bias Step +7 000110_B: DFE Tap-4 Bias Step +6 000101_B: DFE Tap-4 Bias Step +5 000100_B: DFE Tap-4 Bias Step +4 000011_B: DFE Tap-4 Bias Step +3 000010_B: DFE Tap-4 Bias Step +2 000001_B: DFE Tap-4 Bias Step +1 000000_B: DFE Tap-4 Bias Step +0 (Default)	1,2,3
Sign Bit DQU5 DFE Tap-4 Bias	R/W	OP[6]	0_B: Positive DFE Tap-4 Bias (Default) 1_B: Negative DFE Tap-4 Bias	
Enable/Disable DQU5 DFE Tap-4	R/W	OP[7]	0_B: DFE Tap-4 Disable (Default) 1_B: DFE Tap-4 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.155 MR237 through MR239 are undefined.

There a currently no plans to utilize these addresses.

3.5.156 MR240 (MA[7:0]=$F0_H$) - DQU6 DFE VGA - Q3'17 Ballot #1845.62

MR240 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	RFU	RFU	Sign Bit	DQU6 DFE Gain Bias		

Function	Register Type	Operand	Data	Notes
DQU6 DFE Gain Bias	R/W	OP[2:0]	111_B: RFU 101_B: RFU 100_B: RFU 011_B: DFE Gain Bias Step +3 010_B: DFE Gain Bias Step +2 001_B: DFE Gain Bias Step +1 000_B: DFE Gain Bias Step +0 (Default)	1,2,3
Sign Bit DQU6 DFE Gain Bias	R/W	OP[3]	0_B: Positive DFE Gain Bias (Default) 1_B: Negative DFE Gain Bias	
RFU	R/W	OP[7:4]	RFU	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.157 MR241 (MA[7:0]=$F1_H$) - DQU6 DFE Tap-1 - Q3'17 Ballot #1845.62

MR241 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	RFU	DQU6 DFE Tap-1 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU6 DFE Tap-1 Bias	R/W	OP[5:0]	111111_B: RFU : 101001_B: RFU 101000_B: DFE Tap-1 Bias Step +40 100110_B: DFE Tap-1 Bias Step +39 100101_B: DFE Tap-1 Bias Step +38 : 000101_B: DFE Tap-1 Bias Step +5 000100_B: DFE Tap-1 Bias Step +4 000011_B: DFE Tap-1 Bias Step +3 000010_B: DFE Tap-1 Bias Step +2 000001_B: DFE Tap-1 Bias Step +1 000000_B: DFE Tap-1 Bias Step +0 (Default)	1,2,3
Sign Bit DQU6 DFE Tap-1 Bias	R/W	OP[6]	0_B: Positive DFE Tap-1 Bias (Default) 1_B: Negative DFE Tap-1 Bias	
Enable/Disable DQU6 DFE Tap-1	R/W	OP[7]	0_B: DFE Tap-1 Disable (Default) 1_B: DFE Tap-1 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.158 MR242 (MA[7:0]=$F2_H$) - DQU6 DFE Tap-2 - Q3'17 Ballot #1845.62

MR242 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQU6 DFE Tap-2 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU6 DFE Tap-2 Bias	R/W	OP[5:0]	111111_B: RFU : 010000_B: RFU 001111_B: DFE Tap-2 Bias Step +15 001110_B: DFE Tap-2 Bias Step +14 001011_B: DFE Tap-2 Bias Step +13 : 000101_B: DFE Tap-2 Bias Step +5 000100_B: DFE Tap-2 Bias Step +4 000011_B: DFE Tap-2 Bias Step +3 000010_B: DFE Tap-2 Bias Step +2 000001_B: DFE Tap-2 Bias Step +1 000000_B: DFE Tap-2 Bias Step +0 (Default)	1,2,3
Sign Bit DQU6 DFE Tap-2 Bias	R/W	OP[6]	0_B: Positive DFE Tap-2 Bias (Default) 1_B: Negative DFE Tap-2 Bias	
Enable/Disable DQU6 DFE Tap-2	R/W	OP[7]	0_B: DFE Tap-2 Disable (Default) 1_B: DFE Tap-2 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.159 MR243 (MA[7:0]=$F3_H$) - DQU6 DFE Tap-3 - Q3'17 Ballot #1845.62

MR243 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQU6 DFE Tap-3 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU6 DFE Tap-3 Bias	R/W	OP[5:0]	111111_B: RFU : 001011_B: RFU 001010_B: DFE Tap-3 Bias Step +12 001011_B: DFE Tap-3 Bias Step +11 001010_B: DFE Tap-3 Bias Step +10 : 000101_B: DFE Tap-3 Bias Step +5 000100_B: DFE Tap-3 Bias Step +4 000011_B: DFE Tap-3 Bias Step +3 000010_B: DFE Tap-3 Bias Step +2 000001_B: DFE Tap-3 Bias Step +1 000000_B: DFE Tap-3 Bias Step +0 (Default)	1,2,3
Sign Bit DQU6 DFE Tap-3 Bias	R/W	OP[6]	0_B: Positive DFE Tap-3 Bias (Default) 1_B: Negative DFE Tap-3 Bias	
Enable/Disable DQU6 DFE Tap-3	R/W	OP[7]	0_B: DFE Tap-3 Disable (Default) 1_B: DFE Tap-3 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.160 MR244 (MA[7:0]=$F4_H$) - DQU6 DFE Tap-4 - Q3'17 Ballot #1845.62

MR244 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQU6 DFE Tap-4 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU6 DFE Tap-4 Bias	R/W	OP[5:0]	111111_B: RFU : 001001_B: RFU 001000_B: DFE Tap-4 Bias Step +8 000111_B: DFE Tap-4 Bias Step +7 000110_B: DFE Tap-4 Bias Step +6 000101_B: DFE Tap-4 Bias Step +5 000100_B: DFE Tap-4 Bias Step +4 000011_B: DFE Tap-4 Bias Step +3 000010_B: DFE Tap-4 Bias Step +2 000001_B: DFE Tap-4 Bias Step +1 000000_B: DFE Tap-4 Bias Step +0 (Default)	1,2,3
Sign Bit DQU6 DFE Tap-4 Bias	R/W	OP[6]	0_B: Positive DFE Tap-4 Bias (Default) 1_B: Negative DFE Tap-4 Bias	
Enable/Disable DQU6 DFE Tap-4	R/W	OP[7]	0_B: DFE Tap-4 Disable (Default) 1_B: DFE Tap-4 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.161 MR245 through MR247 are undefined.

There a currently no plans to utilize these addresses.

3.5.162 MR248 (MA[7:0]=$F8_H$) - DQU7 DFE VGA - Q3'17 Ballot #1845.62

MR248 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	RFU	RFU	Sign Bit	DQU7 DFE Gain Bias		

Function	Register Type	Operand	Data	Notes
DQU7 DFE Gain Bias	R/W	OP[2:0]	111_B: RFU 101_B: RFU 100_B: RFU 011_B: DFE Gain Bias Step +3 010_B: DFE Gain Bias Step +2 001_B: DFE Gain Bias Step +1 000_B: DFE Gain Bias Step +0 (Default)	1,2,3
Sign Bit DQU7 Gain Bias	R/W	OP[3]	0_B: Positive DFE Gain Bias (Default) 1_B: Negative DFE Gain Bias	
RFU	R/W	OP[7:4]	RFU	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.163 MR249 (MA[7:0]=$F9_H$) - DQU7 DFE Tap-1 - Q3'17 Ballot #1845.62

MR249 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	RFU	DQU7 DFE Tap-1 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU7 DFE Tap-1 Bias	R/W	OP[5:0]	111111_B: RFU : 101001_B: RFU 101000_B: DFE Tap-1 Bias Step +40 100110_B: DFE Tap-1 Bias Step +39 100101_B: DFE Tap-1 Bias Step +38 : 000101_B: DFE Tap-1 Bias Step +5 000100_B: DFE Tap-1 Bias Step +4 000011_B: DFE Tap-1 Bias Step +3 000010_B: DFE Tap-1 Bias Step +2 000001_B: DFE Tap-1 Bias Step +1 000000_B: DFE Tap-1 Bias Step +0 (Default)	1,2,3
Sign Bit DQU7 DFE Tap-1 Bias	R/W	OP[6]	0_B: Positive DFE Tap-1 Bias (Default) 1_B: Negative DFE Tap-1 Bias	
Enable/Disable DQU7 DFE Tap-1	R/W	OP[7]	0_B: DFE Tap-1 Disable (Default) 1_B: DFE Tap-1 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.164 MR250 (MA[7:0]=FA_H) - DQU7 DFE Tap-2 - Q3'17 Ballot #1845.62

MR250 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQU7 DFE Tap-2 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU7 DFE Tap-2 Bias	R/W	OP[5:0]	111111_B: RFU : 010000_B: RFU 001111_B: DFE Tap-2 Bias Step +15 001110_B: DFE Tap-2 Bias Step +14 001011_B: DFE Tap-2 Bias Step +13 : 000101_B: DFE Tap-2 Bias Step +5 000100_B: DFE Tap-2 Bias Step +4 000011_B: DFE Tap-2 Bias Step +3 000010_B: DFE Tap-2 Bias Step +2 000001_B: DFE Tap-2 Bias Step +1 000000_B: DFE Tap-2 Bias Step +0 (Default)	1,2,3
Sign Bit DQU7 DFE Tap-2 Bias	R/W	OP[6]	0_B: Positive DFE Tap-2 Bias (Default) 1_B: Negative DFE Tap-2 Bias	
Enable/Disable DQU7 DFE Tap-2	R/W	OP[7]	0_B: DFE Tap-2 Disable (Default) 1_B: DFE Tap-2 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.165 MR251 (MA[7:0]=FB_H) - DQU7 DFE Tap-3 - Q3'17 Ballot #1845.62

MR251 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQU7 DFE Tap-3 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU7 DFE Tap-3 Bias	R/W	OP[5:0]	111111_B: RFU : 001011_B: RFU 001010_B: DFE Tap-3 Bias Step +12 001011_B: DFE Tap-3 Bias Step +11 001010_B: DFE Tap-3 Bias Step +10 : 000101_B: DFE Tap-3 Bias Step +5 000100_B: DFE Tap-3 Bias Step +4 000011_B: DFE Tap-3 Bias Step +3 000010_B: DFE Tap-3 Bias Step +2 000001_B: DFE Tap-3 Bias Step +1 000000_B: DFE Tap-3 Bias Step +0 (Default)	1,2,3
Sign Bit DQU7 DFE Tap-3 Bias	R/W	OP[6]	0_B: Positive DFE Tap-3 Bias (Default) 1_B: Negative DFE Tap-3 Bias	
Enable/Disable DQU7 DFE Tap-3	R/W	OP[7]	0_B: DFE Tap-3 Disable (Default) 1_B: DFE Tap-3 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.166 MR252 (MA[7:0]=FC_H) - DQU7 DFE Tap-4 - Q3'17 Ballot #1845.62

MR252 Register Information

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enable/ Disable	Sign Bit	DQU7 DFE Tap-4 Bias Programming					

Function	Register Type	Operand	Data	Notes
DQU7 DFE Tap-4 Bias	R/W	OP[5:0]	111111_B: RFU : 001001_B: RFU 001000_B: DFE Tap-4 Bias Step +8 000111_B: DFE Tap-4 Bias Step +7 000110_B: DFE Tap-4 Bias Step +6 000101_B: DFE Tap-4 Bias Step +5 000100_B: DFE Tap-4 Bias Step +4 000011_B: DFE Tap-4 Bias Step +3 000010_B: DFE Tap-4 Bias Step +2 000001_B: DFE Tap-4 Bias Step +1 000000_B: DFE Tap-4 Bias Step +0 (Default)	1,2,3
Sign Bit DQU7 DFE Tap-4 Bias	R/W	OP[6]	0_B: Positive DFE Tap-4 Bias (Default) 1_B: Negative DFE Tap-4 Bias	
Enable/Disable DQU7 DFE Tap-4	R/W	OP[7]	0_B: DFE Tap-4 Disable (Default) 1_B: DFE Tap-4 Enable	

Note 1: Refer to the DDR5 DFE specification for information on Step Size, Step Size Tolerance and Range values
Note 2: The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables
Note 3: The number of step size, step values and range are speed dependent

3.5.167 MR253 through MR255 are undefined.

There a currently no plans to utilize these addresses.

4 DDR5 SDRAM Command Description and Operation

4.1 Command Truth Table - Q3'17 Ballot #1830.42B w/Editorial

(a) Notes 1, 2 & 14 apply to the entire Command truth table
(b) To improve command decode time, the table has been optimized to orient all 1 cycle commands together and all 2 cycle commands together; allowing CA0 & CA1 to be used to identify the difference between a one cycle and a two cycle command.

[BG=Bank Group Address, BA=Bank Address, R=Row Address, C=Column Address, MRA=Mode Register Address, OP=Op Code, CID=Chip ID, CW=Control Word, X=Don't Care, V=Valid].

Table 11 — Command Truth Table

Function	Abbreviation	CS	CA Pins														NOTES
			CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13	
Activate	ACT	L	L	L	R0	R1	R2	R3	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	11,17
		H	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16	CID3/ R17	
RFU	RFU	L	H	L	L	L	L	V	V	V	V	V	V	V	V	V	
		H	V	V	V	V	V	V	V	V	V	V	V	V	V	V	
RFU	RFU	L	H	L	L	L	H	V	V	V	V	V	V	V	V	V	
		H	V	V	V	V	V	V	V	V	V	V	V	V	V	V	
Write Pattern	WRP	L	H	L	L	H	L	H	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	11,15,18,19
		H	V	C3	C4	C5	C6	C7	C8	C9	C10	V	AP=L	H	V	CID3	
RFU	RFU	L	H	L	L	H	H	V	V	V	V	V	V	V	V	V	
		H	V	V	V	V	V	V	V	V	V	V	V	V	V	V	
Mode Register Write	MRW	L	H	L	H	L	L	MRA0	MRA1	MRA2	MRA3	MRA4	MRA5	MRA6	MRA7	V	8,11,13
		H	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	V	V	CW	V	V	V	
Mode Register Read	MRR	L	H	L	H	L	H	MRA0	MRA1	MRA2	MRA3	MRA4	MRA5	MRA6	MRA7	V	8,13
		H	V	V	V	V	V	V	V	V	V	V	CW	V	V	V	
Write	WR	L	H	L	H	H	L	BL*=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	8,12,15,19
		H	V	C3	C4	C5	C6	C7	C8	C9	C10	V	AP=L	WR_ Partial=L	V	CID3	
Read	RD	L	H	L	H	H	H	BL*=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	8,15,19
		H	C2	C3	C4	C5	C6	C7	C8	C9	C10	V	AP=L	V	V	CID3	
Vref CA Command	VrefCA	L	H	H	L	L	L	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	V	
Refresh All	REFab	L	H	H	L	L	H	CID3	V	V	V	V	L	CID0	CID1	CID2	3
Refresh Same Bank	REFsb	L	H	H	L	L	H	CID3	BA0	BA1	V	V	H	CID0	CID1	CID2	4
Precharge All	PREab	L	H	H	L	H	L	CID3	V	V	V	V	L	CID0	CID1	CID2	5
Precharge Same Bank	PREsb	L	H	H	L	H	L	CID3	BA0	BA1	V	V	H	CID0	CID1	CID2	6
Precharge	PREpb	L	H	H	L	H	H	CID3	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	7
RFU	RFU	L	H	H	H	L	L	V	V	V	V	V	V	V	V	V	
Self Refresh Entry	SRE	L	H	H	H	L	H	V	V	V	V	V	L	V	V	V	9
Power Down Entry	PDE	L	H	H	H	L	H	V	V	V	V	V	H	ODT=L	V	V	10,16
MPC	MPC	L	H	H	H	H	L	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	V	
NOP	NOP	L	H	H	H	H	H	V	V	V	V	V	V	V	V	V	
Power Down Exit	PDX	L	H	H	H	H	H	V	V	V	V	V	V	V	V	V	
Deselect	DES	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	

1. V means H or L (a defined logic level). X means don't care in which case the signal may be floated.
2. Bank group addresses BG[2:0] and Bank addresses BA[1:0] determine which bank is to be operated upon in a specific bank group.
3. The Refresh All command is applied to all banks in all bank groups. The bank addresses and bank group addresses are don't care.
4. The Refresh Same Bank command refreshes the same bank in all bank groups. The bank bits specify the bank within each bank group.
5. The Precharge All command applies to all open banks in all bank groups.
6. The Precharge Same Bank command applies to the same bank in all bank groups. The bank bits specify the bank within each bank group.
7. The Precharge command applies to a single bank as specified by bank address and bank group bits.
8. CS=LOW during the 2nd cycle of a two cycle command controls ODT in non-target ranks for WR, RD and MRR commands, and to MRW commands when in PDA mode.
9. The SRE command places the DRAM in self refresh state
10. The PDE command places the DRAM in power down state
11. Two cycle commands with no ODT control (ACT, MRW not in PDA mode, WRP). DRAM does not execute the command if it receives CS as LOW on 2nd cycle
12. WR command with WR_partial = Low indicates a partial write command. This is to help DRAM start an internal read for 'read modify write'.
13. If CW=LOW during MRR and MRW commands then DRAM should execute commands. If CW=HIGH then DRAM ignores MRR and MRW commands, but still drives the strobes during MRR as if data were still being sent.
14. CID[3:0] bits are used for 3DS stacking support.
15. If CA5:BL*=L, the command places the DRAM into the alternate Burst mode described by MR0[1:0] instead of the default Burst Length 16 mode.
16. ODT=L is defined to allow On Die Termination (ODT) to persist when the device is in Power Down Mode.
17. CID3/R17 is a multi-mode pin allowing for either 16H 3DS stacking with the CID3 bit usage or R17 for high bit density monolithic usage. These usages are mutually exclusive.
18. Write Pattern only supports BL16.
19. When CID3 is not used, it's CA decode is VALID.

4.2 Burst Length, Type and Order - Q2'16 Ballot #1830.43 w/Editorial Updates

Accesses within a given burst is currently limited to only sequential, interleaved is not supported. The ordering of accesses within a burst is determined by the burst length and the starting column address as shown in Table 12. The burst length is defined by bits OP[1:0] of Mode Register MR0. Burst length options include BC8 OTF, BL16, BL32 (optional) and BL32 OTF.

Table 12 — Burst Type and Burst Order for READ

Burst Length	Burst Type	C3	C2	C1	C0	Read Burst Cycle and Burst Address Sequence															
						1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**
BC8	SEQ	0	0	V	V	0	1	2	3	4	5	6	7	T	T	T	T	T	T	T	T
		0	1	V	V	4	5	6	7	0	1	2	3	T	T	T	T	T	T	T	T
		1	0	V	V	8	9	A	B	C	D	E	F	T	T	T	T	T	T	T	T
		1	1	V	V	C	D	E	F	8	9	A	B	T	T	T	T	T	T	T	T
BL16	SEQ	0	0	V	V	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		0	1	V	V	4	5	6	7	0	1	2	3	C	D	E	F	8	9	A	B
		1	0	V	V	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
		1	1	V	V	C	D	E	F	8	9	A	B	4	5	6	7	0	1	2	3

Table 13 — Burst Type and Burst Order for WRITE

Burst Length	Burst Type	C3	C2	C1	C0	Write Burst Cycle and Burst Address Sequence															
						1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**
BC8	SEQ	0	V	V	V	0	1	2	3	4	5	6	7	X	X	X	X	X	X	X	X
		1	V	V	V	8	9	A	B	C	D	E	F	X	X	X	X	X	X	X	X
BL16	SEQ	0	V	V	V	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

NOTE 1 In case of burst length being fixed to 8 by MR[TBD] setting, the internal write operation starts four clock cycles earlier than for the BL16 mode. This means that the starting point for tWR and tWTR will be pulled in by four clocks.
NOTE 2 T: Output driver for data and strobes are in high impedance.
NOTE 3 V : A valid logic level (0 or 1), but respective buffer input ignores level on input pins.
NOTE 4 X : Don't Care.

4.3 Precharge Command - Q3'17 Ballot #1845.60

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time (tRP) after the PRECHARGE command is issued, except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

If CA10 on the 2nd pulse of a Read or Write command is LOW, (shown as AP=L in the command truth table) then the auto-precharge function is engaged. This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon CAS latency) thus improving system performance for random data access. The RAS lockout circuit internally delays the precharge operation until the array restore operation has been completed (tRAS satisfied) so that the auto precharge command may be issued with any read. Auto-precharge is also implemented during Write commands. The precharge operation engaged by the Auto precharge command will not begin until the last data of the burst write sequence is properly stored in the memory array. The bank will be available for a subsequent row activation a specified time (tRP) after hidden PRECHARGE command (AutoPrecharge) is issued to that bank. The precharge to precharge delay is defined by tPPD in the core timing tables.

4.3.1 Precharge Command Modes

DDR5 supports three different types of precharge commands: Precharge, Precharge All and Precharge Same Bank

The Precharge Command (PREpb) applies precharge to a specific bank defined by BA[1:0] {if applicable} in a specific bank group defined by BG[2:0], while a Precharge All (PREab) applies precharge to all banks in all bank groups and a Precharge Same Bank (PREsb) applies precharge to a specific bank defined by BA[1:0] in all bank groups. In the case of a 3DS DDR5 SDRAM device, CID[3:0] will also be selected to identify the target die.

Table 14 below shows the different encodes for PREpb, PREab and PREsb.

Table 14 — Precharge Encodings

Function	Abbreviation	CS	CA Pins														NOTES
			CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13	
Precharge All	PREab	L	H	H	L	H	L	CID3	V	V	V	V	L	CID0	CID1	CID2	
Precharge Same Bank	PREsb	L	H	H	L	H	L	CID3	BA0	BA1	V	V	H	CID0	CID1	CID2	
Precharge	PREpb	L	H	H	L	H	H	CID3	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	

NOTE: Refer to command truth table for details.

4.4 Activate Command - Q3'17 Ballot #1845.23A

The ACTIVATE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BG[2:0] in X4/8 and BG[1:0] in X16 select the bankgroup; BA[1:0] inputs selects the bank within the bankgroup, and the address provided on the appropriate CA pins for R[17:0] to select the row (see table 1 below). In the case of a 3DS DDR5 SDRAM device, the CID[3:0] will also be selected to identify the correct die in the stack. This row remains active (or open) for accesses until a precharge command is issued to that bank or a precharge all command is issued. A bank must be precharged before opening a different row in the same bank.

Table 15 — Activate Command (for reference)

Function	Abbreviation	CS	CA Pins													NOTES
			CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13	
Activate	ACT	L	L	L	R0	R1	R2	R3	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	1
		H	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16	CID3/ R17	

Note 1 - See Command Truth Table for details

REFERENCE NOTE - DDPID not shown on CA13 encoding - this ballot needs to get updated to reflect DDP support. See command truth table for details.

4.5 Read Operation - No Ballot

4.5.1 READ Timing Definitions - No Ballot

Read timing shown in this section is applied when the DLL is enabled and locked.

4.5.1.1 CLK to Read DQS timing parameters - Q1'17 Ballot #1830.75A

Following parameters will be defined for CK to read DQS timings.

Table 16 — CLK to Read DQS Timing Parameters

Speed		DDR5-3200/3600/4000/4400		Units	NOTE
Parameter	Symbol	Min	Max		
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c	tDQSCK	TBD	TBD	ps	1,4,5
DQS_t, DQS_c rising edge output variance window	tDQSCKi	-	TBD	ps	2,3,4,5

NOTE 1 Measured over full VDD and Temperature spec ranges.
NOTE 2 Measured for a given DRAM part, and for each DQS_t/DQS_c pair in case of x16 (part variation is excluded).
NOTE 3 These parameters are verified by design and characterization, and may not be subject to production test.
NOTE 4 Assume no jitter on input clock signals to the DRAM.
NOTE 5 Refer to Section 4.7.1 READ Timing Definitions.

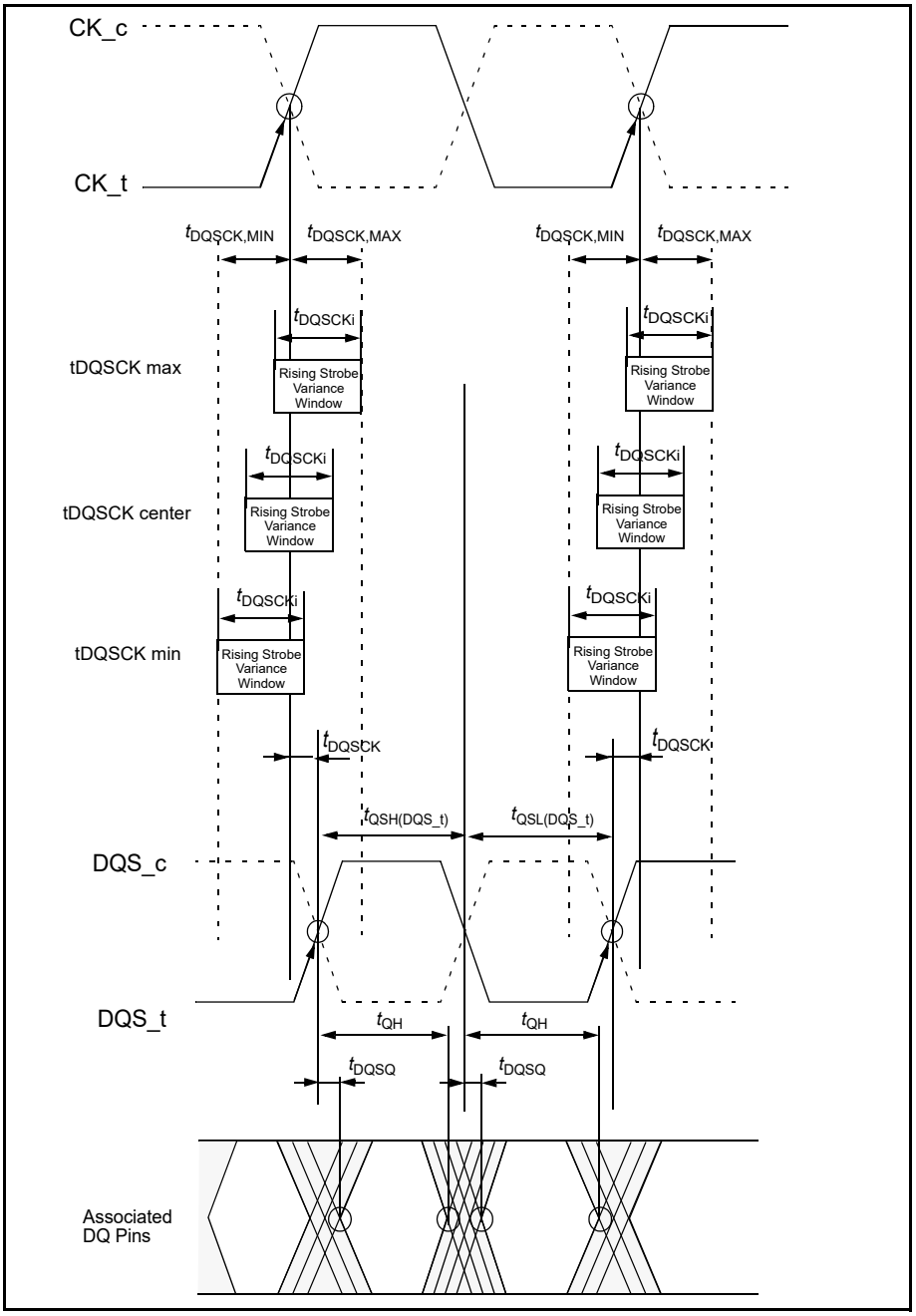


Figure 7 — TDQSCK Timing Definition

4.6 Write Operation - No Ballot

4.6.1 Write Timing Parameters - No Ballot

This drawing is for example only to enumerate the strobe edges that “belong” to a Write burst. No actual timing violations are shown here. For a valid burst all timing parameters for each edge of a burst need to be satisfied (not only for one edge - as shown).

TBD

Figure 8 — Write Timing Definition and Parameters with 1tCK Preamble

TBD

Figure 9 — Write Timing Definition and Parameters with 2tCK Preamble

4.6.2 Write Data Mask - No Ballot

One write data mask (DM_n) pin for each 8 data bits (DQ) will be supported on DDR5 SDRAMs, consistent with the implementation on DDR3 SDRAMs. It has identical timings on write operations as the data bits as shown in Figure AA and BB, and though used in a unidirectional manner, is internally loaded identically to data bits to ensure matched system timing. DM_n is not used during read cycles for any bit organizations including x4, x8, and x16, however, DM_n of x8 bit organization can be used as TDQS_t during write cycles if enabled by the MR1[A11] setting and x8 /x16 organization as DBI_n during write cycles if enabled by the MR5[A11] setting. See “TDQS_t, TDQS_c” on page TBD for more details on TDQS vs. DM_n operations and DBI_n on page TBD for more detail on DBI_n vs. DM_n operations.

4.6.3 tWPRE Calculation - No Ballot

4.6.4 Write Burst Operation - No Ballot

The following write timing diagram is to help understanding of each write parameter's meaning and just examples. The details of the definition of each parameter will be defined separately.
In these write timing diagram, CK and DQS are shown aligned and also DQS and DQ are shown center aligned for illustration purpose.

4.6.5 Read and Write Command Interval - No Ballot

Bank Group	Timing Parameter	DDR5-3200 / 3733 / 4266 / 5333 / 6400	Units	note
same	Minimum Read to Write	CL - CWL + RBL / 2 + 1 tCK + tWPRE		1, 2
	Minimum Read after Write	CWL + WBL / 2 + tWTR_L		1, 3
different	Minimum Read to Write	CL - CWL + RBL / 2 + 1 tCK + tWPRE		1, 2
	Minimum Read after Write	CWL + WBL / 2 + tWTR_S		1, 3

Table 17 — Minumum Read and Write Command Timings

NOTE:
1. These timings require extended calibrations times tZQinit and tZQCS.
2. RBL : Read burst length associated with Read command
RBL = 8 for fixed 8 and on-the-fly mode 8
RBL = 4 for fixed BC4 and on-the-fly mode BC4
3. WBL : Write burst length associated with Write command
WBL = 8 for fixed 8 and on-the-fly mode 8 or BC4
WBL = 4 for fixed BC4 only

4.6.6 Write Timing Violations - No Ballot

4.7 Self Refresh Operation - Q3'17 Ballot #1830.46A

The Self-Refresh command can be used to retain data in the DDR5 SDRAM, even if the rest of the system is powered down. When in the Self-Refresh mode, the DDR5 SDRAM retains data without external clocking.The DDR5 SDRAM device has a built-in timer to accommodate Self-Refresh operation.

Self Refresh entry is command based (SRE), while the Self-Refresh Exit Command is defined by the transition of CS_n LOW to HIGH with a defined pulse width tCSH, followed by three NOP commands to ensure DRAM stability in recognizing the exit. This is described below in more detail.

Before issuing the Self-Refresh-Entry command, the DDR5 SDRAM must be idle with all bank precharge state with tRP satisfied. 'Idle state' is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, and all timings from previous operations are satisfied (tMRD, tMRRI, tRFC, tZQxxx, etc.). A Deselect command must be registered on the last positive clock edge before issuing Self Refresh Entry command. Once the Self Refresh Entry command is registered, Deselect commands must also be registered at the next positive clock edges until tCPDED is satisfied. After tCPDED has been satisfied, CS_n must transition low. After CS_n transitions low at the end of tCPDED, the CS_n will stay low until exit. The DDR5 SDRAM may switch to a CMOS based receiver to save more power and that transition should coincide with CS_n going low.

When the CS_n is held low, the DRAM automatically disables ODT termination and sets Hi-Z as termination state regardless RTT configuration for the duration of Self-Refresh mode. Upon exiting Self-Refresh, DRAM automatically enables ODT termination and set RTT_PARK (for DQs) asynchronously during tXSDLL when RTT_PARK is enabled. CA/CS/CK ODT will revert to its strapped or its MR ODT Setting state if previously applied. During normal operation (DLL on) the DLL is automatically disabled upon entering Self-Refresh and is automatically enabled (including a DLL-Reset) upon exiting Self-Refresh.

When the DDR5 SDRAM has entered Self-Refresh mode, all of the external control signals, except CS_n and RESET_n, are "don't care." For proper Self-Refresh operation, all power supply and reference pins (VDD, VDDQ, VSS, VSSQ and VPP) must be at valid levels. DRAM internal VrefDQ and/or VrefCA generator circuitry may remain ON or turned OFF depending on DRAM design. If DRAM internal VrefDQ and/or VrefCA circuitry is turned OFF in self refresh, when DRAM exits from self refresh state, it ensures that VrefDQ and/or VrefCA and generator circuitry is powered up and stable within tXS period. First Write operation or first Write Leveling Activity may not occur earlier than tXS after exit from Self Refresh. The DRAM initiates a minimum of one Refresh command internally within tSR period once it enters Self-Refresh mode.

The clocks must stay on until tCKLCS but can be DON'T CARE after tCKLCS expires but it should be noted that shortly after tCPDED, the termination for the clocks will be off. The clock is internally disabled (in the DRAM) during Self-Refresh Operation to save power. The minimum time that the DDR5 SDRAM must remain in Self-Refresh mode is tCSSR. The user may change the external clock frequency or halt the external clock tCKLCS after Self-Refresh entry is registered, however, the clock must be restarted and stable tCKSRX before the device can exit Self-Refresh operation.

The procedure for exiting Self-Refresh requires a sequence of events. Since the DRAM will switch to a CMOS based driver to save power, the DRAM will trigger Self-Refresh exit upon seeing the CS_n transition from low to high and stay high for tCSH. tCASRX prior to CS_n transitioning high, the CA bus must be driven high. Once tCSH is satisfied, three NOP commands must be issued. The clocks must be valid for tCKSRX prior to issuing the NOP commands that completes the Self Refresh exit sequence. Once a Self-Refresh Exit is registered, the following timing delay must be satisfied:

1. Commands that do not require locked DLL:
tXS - ACT, PRE, REF, SRE, PDE, WRP
tXSFast - ZQStart, ZQLatch.

2. Commands that require locked DLL:
tXSDLL - RD, WL, WR, MRR, MRW
Depending on the system environment and the amount of time spent in Self-Refresh, ZQ calibration commands may be required to compensate for the voltage and temperature drift as described in "ZQ Calibration Commands". To issue ZQ calibration commands, applicable timing requirements must be satisfied.

The use of Self-Refresh mode introduces the possibility that an internally timed refresh event can be missed when CS_n is pulsed for exit from Self-Refresh mode. Upon exit from Self-Refresh, the DDR5 SDRAM requires a minimum of one extra refresh command before it is put back into Self-Refresh Mode.

The exit timing from self-refresh exit to first valid command not requiring a locked DLL is tXS.
The value of tXS is (tRFC+10ns). This delay is to allow for any refreshes started by the DRAM to complete. tRFC continues to grow with higher density devices so tXS will grow as well.

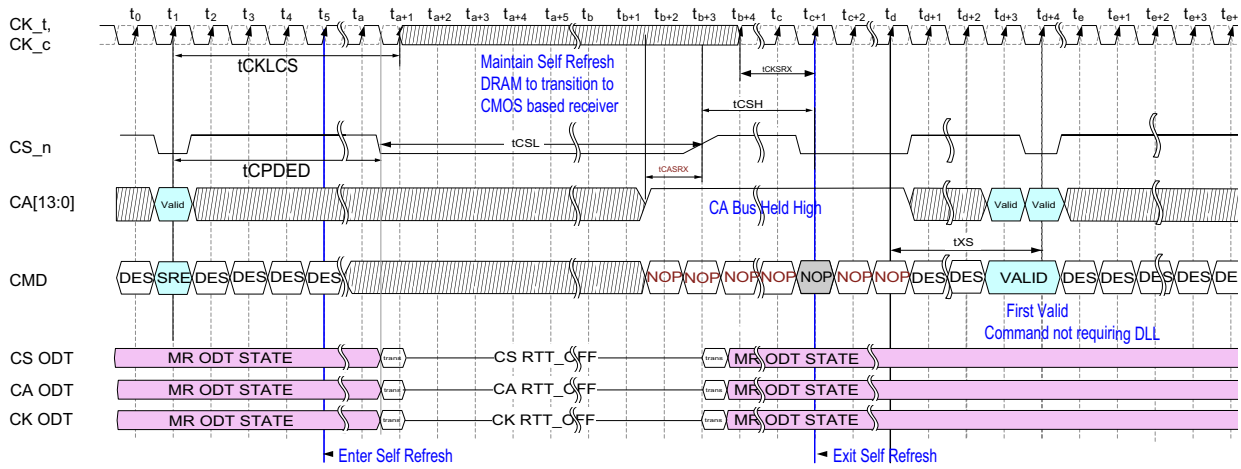


Figure 10 — Self-Refresh Entry/Exit Timing

Table 18 — Self-Refresh Timing Parameters

Parameter	Symbol	Min	Max	Unit	Note
Command pass disable delay	tCPDED	5	-	ns	
Self-Refresh CS_n low Pulse width	tCSL	10	-	ns	
Self-Refresh exit CS_n High Pulse width	tCSH	10	15	ns	
Valid Clock Requirement before SRX	tCKSRX	2.5	5	ns	
Valid Clock Requirement after SRE	tCKLCS	tCPDED + 1nCK	-		
Self-Refresh exit CS_n high	tCASRX	0		ns	
Exit Self-Refresh to next valid command not requireing DLL	tXS	tRFC		ns	

4.8 Power down Mode - Q3'17 Ballot #1830.46A

DDR5's power down mode is new to the DDR family, as it no longer has a CKE pin to control entry and exit. Instead, the PDE/PDX move to command based, triggered by the CS_n. Once in PD mode, the CS_n acts effectively like the historic CKE pin, waiting for it to transition from HIGH to LOW (with its command). In PDE mode, it should be sampled on every edge.

4.8.1 Power-Down Entry and Exit

Power-down is entered when the command is registered. Unlike Self Refresh Mode, CS_n will NOT be held low constantly while in Power-Down. Timing diagrams are shown in Figure 147 through Figure 155 with details for entry and exit of Power-Down.

The DLL should be in a locked state when power-down is entered for fastest power-down exit timing. SDRAM design provides all AC and DC timing and voltage specification as well as proper DLL operation as long as DRAM controller complies with SDRAM specifications.

During Power-Down, if all banks are closed after any in-progress commands are completed, the device will be in precharge Power-Down mode; if any bank is open after in-progress commands are completed, the device will be in active Power-Down mode.

Entering power-down deactivates the input and output buffers, excluding CK_t, CK_c, CS_n, RESET_n. If CA11=L during the PDE command, CA1 and CA4 will also be excluded, allowing the appropriate NT ODT command to be passed through and decoded by the non-target SDRAM while the target SDRAM remains in power down (i.e. the SDRAM will monitor commands that utilize NT ODT via CA1 and CA4 and will not exit Power Down if a valid NT ODT command is registered). If CA11=H during the PDE command, only the PDX command, qualified by CS_n, is legal during power down. If CA11=L during the PDE command, only NT ODT commands and PDX commands, qualified by CS_n, are legal during power down. Refer to the command truth table for more information.

To protect SDRAM internal delay on decoding the Power-Down command, multiple Deselect commands are needed after, this timing period are defined as tCPDED. PDE will result in deactivation of command and address receivers after tCPDED has expired.

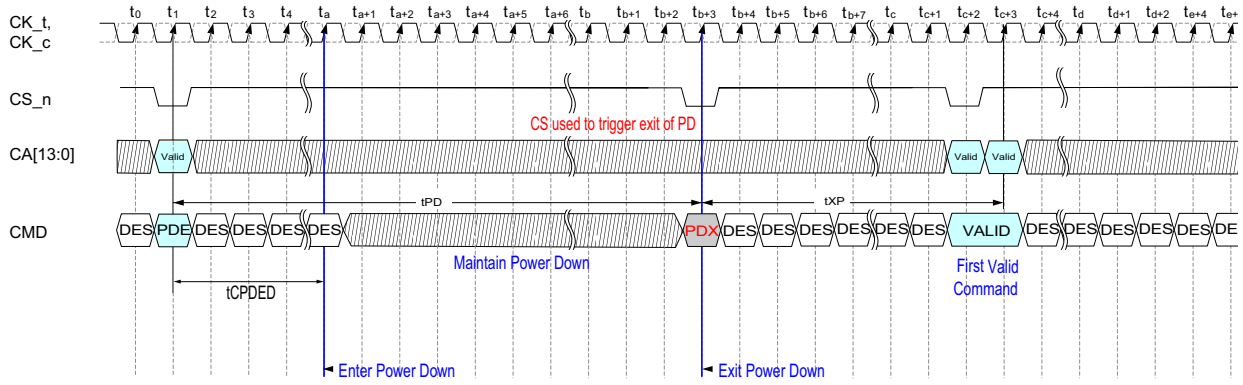


Figure 11 — Power-Down Entry and Exit Mode

Table 19 — Power-Down Entry Definitions

Status of DRAM	DLL	PD Exit	Relevant Parameters
Active (A bank or more Open)	On	Fast	tXP to any valid command
Precharged (All banks Precharged)	On	Fast	tXP to any valid command.

The DLL is kept enabled during precharge power-down or active power-down. (If RESET_n goes low during Power-Down, the DRAM will be out of PD mode and into reset state). Power-down duration is limited by 9 times tREFI of the device.

Power-down exit latency is defined in the AC specifications Table in Section x

Table 20 — Valid Command During Power Down with ODT enabled

CA1	CA4	Command	Operation of DRAM in Power Down
L	L	Write	DRAM will enable ODT_WR_NOM
L	H	Read	DRAM will enable ODT_RD_NOM
H	L	Illegal	Illegal. CS will NOT be asserted to a powered down DRAM with this combination
H	H	PDX(NOP)	Exit Power Down

NOTE: BL bit is observed to determine the timing of the termination if Burst on the Fly is enabled.

4.9 Maximum Power Saving Mode (MPSM) - Q2'17 Ballot #1845.29A w/Editorial Update

When Maximum Power Saving Mode is enabled by setting the MPSM enable (MR3:OP[1]) bit to '1' using MRW command, the device enters Maximum Power Saving Mode Idle (MPSM Idle) state. Once the DRAM is placed into the MPSM Idle state, it can stay in that state indefinitely, or it can further enter either Maximum Power Saving Mode Power Down (MPSM Power Down) state or Maximum Power Saving Mode Self Refresh (MPSM Self Refresh) state.

Data retention is not guaranteed when DRAM is in any of MPSM states. Mode register status and Soft PPR informations are preserved.

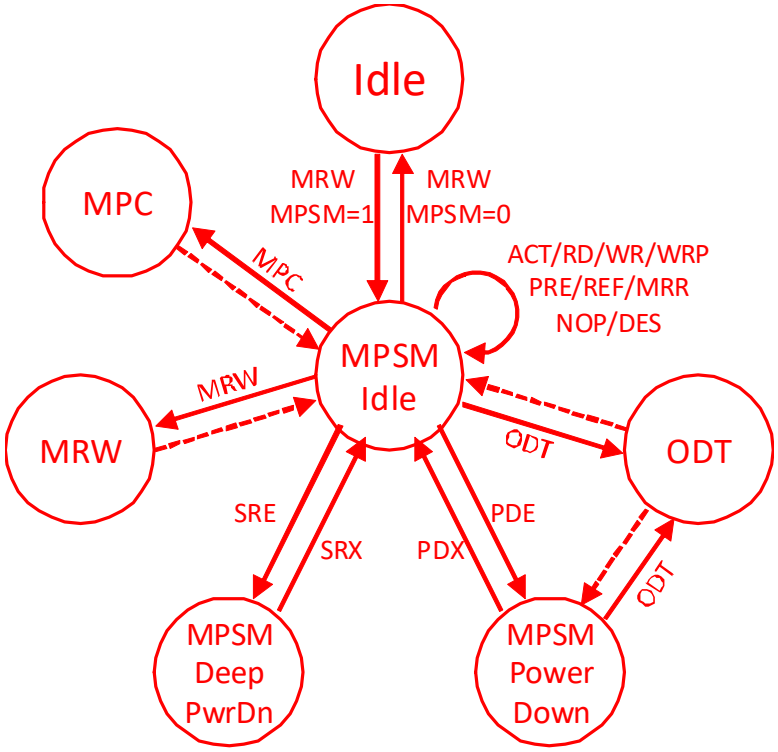


Figure 12 — State diagram for Maximum Power Saving Mode

4.9.1 MPSM Idle State

When DDR5 SDRAM is in this state, it ignores all types of commands except MRW, MPC, ODT, Power Down Entry (PDE) and Self Refresh Entry (SRE) commands. MRW, MPC, ODT, PDE and SRE commands are executed normally. DRAM shall not respond to any other command except these five command types. DLL status is same as in normal idle state.

Normal command timing parameters are applied in this state, except that tREFI doesn't need to be satisfied as Refresh command doesn't need to be issued in this state.

4.9.2 MPSM Power Down State

MPSM Power Down state is entered by Power Down Entry command from MPSM Idle state. When DDR5 SDRAM is in this state, it responds to ODT command normally as it does in precharged power down state. DLL status is same as in normal precharged power down state.

When Power Down Exit command is issued, DRAM goes back to the MPSM Idle state.
Normal Power Down command timings are applied in this state, except the tREFI requirement.

4.9.3 MPSM Deep Power Down State

MPSM Deep Power Down (DPD) state is entered and exited by Self Refresh Entry and Exit commands from/to MPSM Idle state. Input signal requirements to the DRAM in this state are same to those in the Self Refresh mode. DRAM shall not execute any internal Refresh operation in this state.

Normal Self Refresh command timings are applied in this state.

4.9.4 MPSM command timings

The device can exit from the MPSM Idle state by programming the MPSM enable (MR3:OP[1]) bit to '0' using MRW command.
MPSM Idle state exit (MRW) command to the first valid command delay (tMPSMX) is same to normal tMOD.
Minimum delay from MPSM Deep Power Down state exit to the first Activation command is tMPSMX.

Table 21 — Maximum Power Saving Mode Timing Parameters

Symbol	Description	min	max	unit
tMPSMX	MPSM exit to first valid command delay	tMOD	-	ns
tMPDPDACT	MPSM DPD exit to first ACT command delay	TBD	-	ns

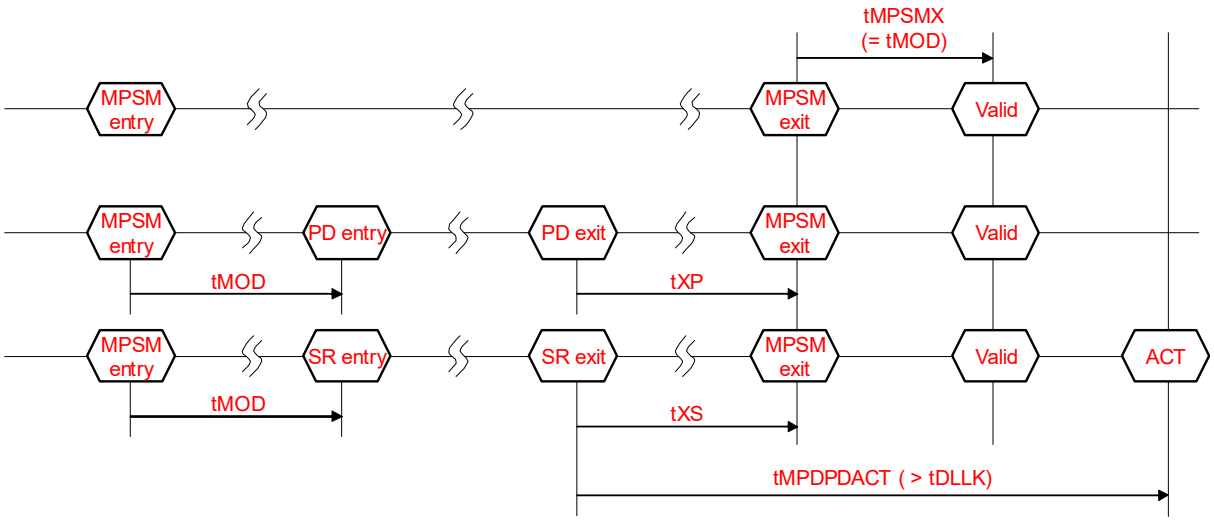


Figure 13 — Maximum Power Saving Mode exit timings

4.10 Refresh Operation - Q3'17 Ballot # 1830.93A

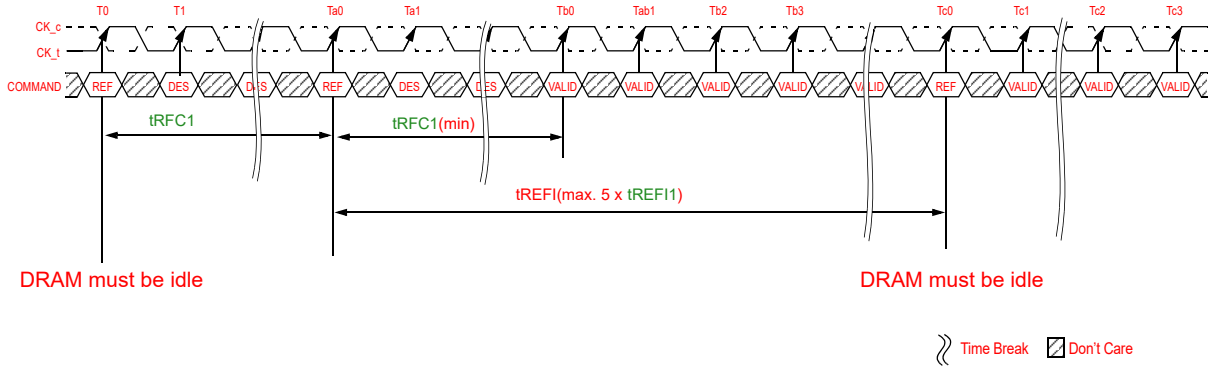
The Refresh command (REF) is used during normal operation of the DDR5 SDRAMs. This command is non persistent, so it must be issued each time a refresh is required. The DDR5 SDRAM requires Refresh cycles at an average periodic interval of tREFI.

There are three types of refresh operations supported by DDR5 SDRAMs.

- Normal Refresh: By issuing All Bank Refresh (REFab) command in Normal Refresh mode
- Fine Granularity Refresh: By issuing All Bank Refresh (REFab) command in Fine Granularity Refresh mode
- Same Bank Refresh: By issuing Same Bank Refresh (REFsb) command in Fine Granularity Refresh mode

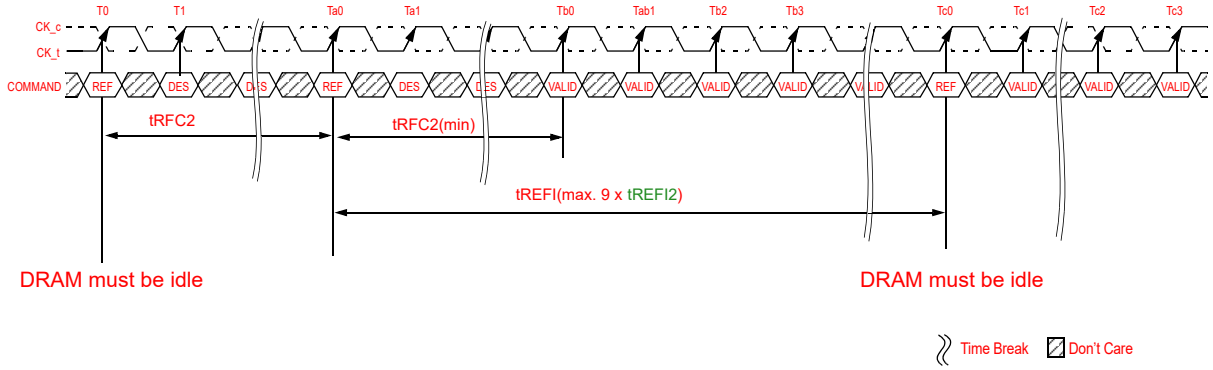
This section describes the details of the refresh operations and requirements for each of the refresh operation types as well as the transitions between the refresh operation types.

For Normal Refresh and Fine Granularity Refresh operations, all banks of the SDRAM must be precharged and idle for a minimum of the precharge time tRP(min) before the Refresh command (REFab) can be issued. The refresh addressing is generated by the internal refresh controller during the refresh cycle. The external address bus is only required to be in a valid state once this cycle has started. When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Refresh command and the next valid command, except DES and non-Target ODT commands, must be greater than or equal to the minimum Refresh cycle time tRFC(min) as shown in Figure 14 and Figure 2. Note that the tRFC timing parameter depends on memory density and the refresh mode setting, which can be set to Normal Refresh mode or Fine Granularity Refresh (FGR) mode.



NOTE: 1. Only DES or non-Target ODT commands are allowed after Refresh command is issued until tRFC1(min) expires.
2. Time interval between two Refresh commands may be extended to a maximum of 5 x tREFI1.

Figure 14 — Refresh Command Timing (Example of Normal Refresh Mode)



NOTE: 1. Only DES or non-Target ODT commands are allowed after Refresh command is issued until tRFC2(min) expires.
2. Time interval between two Refresh commands may be extended to a maximum of 9 x tREFI2.

Figure 15 — Refresh Command Timing (Example of Fine Granularity Refresh Mode)

4.10.1 Refresh Modes

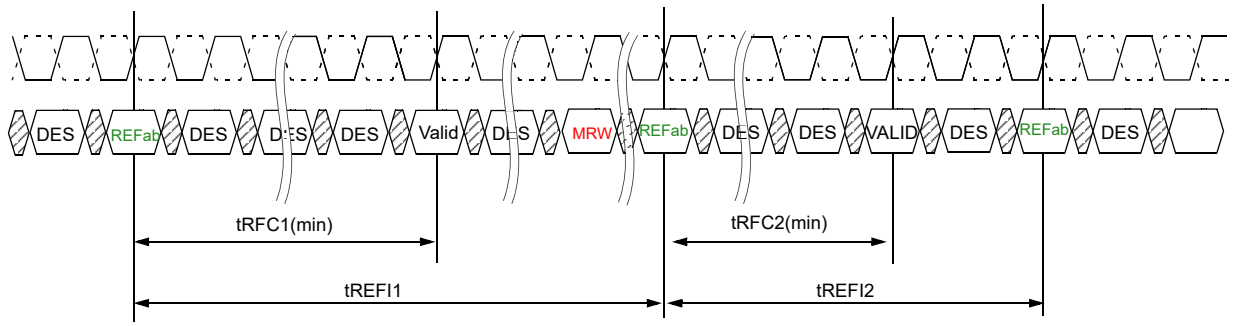
The DDR5 SDRAM has two different Refresh modes with two different refresh cycle time (tRFC) settings. There is a Normal Refresh mode setting and a Fine Granularity Refresh (FGR) mode setting. The FGR mode provides a shorter refresh cycle time (tRFC2) but also requires Refresh commands (REFab) to be provided twice as often (tREFI is divided by two, i.e. tREFI2 = tREFI1/2). The Refresh mode setting is programed by MRW command as shown in Table 22. The Refresh Modes are fixed until changed by MRW command to MR4 OP[4]. No on-the-fly Refresh mode change is supported.

Table 22 — Mode Register definition for Refresh Mode

MR4 OP[4]	Refresh Mode (tRFC setting)
0	Normal Refresh Mode (tRFC1)
1	Fine Granularity Refresh Mode (tRFC2)

4.10.2 Changing Refresh Mode

If Refresh Mode is changed by MRW, the new tREFI and tRFC parameters would be applied from the moment of the rate change. As shown in Figure 16, when a Refresh command is issued to the DRAM in Normal Refresh mode, then tRFC1 and tREFI1 are applied from the time that the command (REFab) was issued. And when a Refresh command is issued in Fine Granularity Refresh (FGR) mode, then tRFC2 and tREFI2 should be satisfied.



NOTE: 1. Refresh mode is Normal Refresh mode before the MRW and FGR mode after the MRW

Figure 16 — Refresh Mode Change Command Timing

The following conditions must be satisfied before the Refresh mode can be changed. Otherwise, data retention of DDR5 SDRAM cannot be guaranteed.

1. In the Normal Refresh mode, the REFab command must complete and tRFC1 must be satisfied before issuing the MRW command to change the Refresh Mode.

2. In the Fine Granularity Refresh mode, it is recommended that an even number of REFab commands are issued to the DDR5 SDRAM since the last change of the Refresh mode with an MRW command before the Refresh mode is changed again by another MRW command. If this condition is met, no additional Refresh commands are required upon the Refresh mode change. If this condition is not met, one extra REFab command is required to be issued to the DDR5 SDRAM upon Refresh mode change. This extra Refresh command is not counted toward the computation of the average refresh interval (tREFI).

4.10.3 Same Bank Refresh

Same Bank Refresh command (REFsb) allows the DDR5 DRAM to apply the refresh process to a specific bank in each bank group unlike the All Bank Refresh command (REFab) which applies the refresh process to all banks in every bank group. The determination whether a Same Bank Refresh or an All Bank Refresh is executed by the DRAM depends on whether REFsb or REFab command is issued, as shown in the command truth table. The REFsb command is only allowed in FGR mode (MR4[OP4]=1).

Each Same Bank Refresh command (REFsb) increments an internal bank counter and once the bank counter equals the number of available banks in a bank group, it will reset and start over on the next subsequent REFsb. Each time the internal bank counter resets and starts over on the next subsequent REFsb, the global refresh counter will also increment. A REFsb command can be issued to any bank and in any bank order. However, every bank must have one REFsb command issued to it before any bank may be issued a subsequent REFsb command; thus, a subsequent REFsb command issued to the same bank prior to every bank receiving a REFsb command is illegal. The first REFsb command issued is the “Synchronization” REFsb command and the “Synchronization” count resets the internal bank counter to zero when either (a) every bank has received one REFsb command, (b) RESET is applied, (c) entering/exiting self refresh mode, or (d) REFab is issued. The DRAM’s global refresh counter increments when either a REFab is issued or when all banks have received their one REFsb command and the “Synchronization” count reset to zero. If a REFab command issued when the bank counter is not zero, i.e. in the middle of same-bank refreshing, the SDRAM’s global refresh counter will not increment.

The REFsb command must not be issued to the device until the following conditions are met:

-tRFC1 or tRFC2 has been satisfied after the prior 1x or 2x REFab command(s), respectively

-tRFCsb has been satisfied after the prior REFsb command

-tRP has been satisfied after the prior PRECHARGE command to that bank

-tRRD_L has been satisfied after the prior ACTIVATE command (e.g. tRRD_L has to be met from ACTIVATE of a different bank in the same bank group to the REFsb targeted at the same bank group)

Once a REFsb is issued, the target banks (one in each Bank Group) are inaccessible during the same-bank refresh cycle time (tRFCsb); however, the other banks in each bank group are accessible and can be addressed during this same-bank refresh cycle. When the same-bank refresh cycle has completed, the banks refreshed via the REFsb will be in idle state.

After issuing REFsb command, the following conditions must be met:

-tRFCsb must be satisfied before issuing a REFab command

-tRFCsb must be satisfied before issuing an ACTIVATE command to the same bank

-tREFSBRD must be satisfied before issuing an ACTIVATE command to a different bank.

Table 23 — Refresh command scheduling separation requirements

Symbol	Min Delay From	To	NOTE
tRFC1	REFab	REFab	1
		ACTIVATE command to any bank	
tRFC2	REFab	REFab	2
		ACTIVATE command to any bank	
		REFsb	
tRFCsb	REFsb	REFab	2
		ACTIVATE command to same bank as REFsb	
		REFsb	
tREFSBRD	REFsb	ACTIVATE command to different bank from REFsb	2
tRRD_L	ACTIVATE	REFsb to different bank from ACTIVATE	2

NOTES:

1 - MR4(OP[4]) set to Normal Refresh mode.

2 - MR4(OP[4]) set to FGR mode. REFsb command is valid only in FGR mode.

A single REFab command can be replaced with 2 or 4 REFsb commands for purpose of scheduling in terms of postponing and pulling in of refresh commands. Each burst REFsb limitation is governed by 4 x (tRFCsb + [(n-1) x tRRD_L]) where n= number of banks in a bank group.

4.10.4 tREFI and tRFC parameters

The maximum average refresh interval (tREFI) requirement for the DDR5 SDRAM depends on the refresh mode setting (Normal or FGR), and the device's case temperature (Tcase). When the refresh mode is set to Normal Refresh mode (tRFC1), and Tcase<=85°C, the maximum average refresh interval (tREFI1) is tREFI. When the refresh mode is set to FGR mode (tRFC2) and Tcase<=85°C, the maximum average refresh interval (tREFI2) is tREFI/2. This same tREFI/2 interval value is also appropriate if the refresh mode is set to Normal Refresh mode (tRFC1) but 85°C<Tcase<=95°C. Finally, if the refresh mode is set to FGR mode (tRFC2) and 85°C<Tcase<=95°C the maximum average refresh interval (tREFI2) is tREFI/4.

Table 24 — tREFI parameters for REFab Command by device density

Refresh Mode	Parameter		Expression	Value	Unit
Normal	tREFI1	0°C <= TCASE <= 85°C	tREFI	3.9	us
		85°C < TCASE <= 95°C	tREFI/2	1.95	us
Fine Granularity	tREFI2	0°C <= TCASE <= 85°C	tREFI/2	1.95	us
		85°C < TCASE <= 95°C	tREFI/4	0.975	us

Table 25 — tRFC parameters

Refresh Operation	Parameter	8Gb	16Gb	32Gb	Units
Normal Refresh (REFab)	tRFC1(min)	195	295	TBD	ns
Fine Granularity Refresh (REFab)	tRFC2(min)	130	160	TBD	ns
Same Bank Refresh (REFsb)	tRFCsb(min)	115	130	TBD	ns

Table 26 — Same Bank Refresh parameter

Refresh Mode	Parameter	8Gb	16Gb	32Gb	Units
Same Bank Refresh to ACT delay	tREFSBRD(min)	30	30	TBD	ns

4.10.5 Refresh Operation Scheduling Flexibility

In general, a Refresh command needs to be issued to the DDR5 SDRAM regularly every tREFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided for postponing and pulling in refresh command.

In Normal Refresh mode, a maximum of 4 Refresh commands can be postponed, meaning that at no point in time more than a total of 4 Refresh commands are allowed to be postponed. In case that 4 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to 5 × tREFI1 (see Figure 3). A maximum of 4 additional Refresh commands can be issued in advance (“pulled in”), with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 4 Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to 5 × tREFI1 (see Figure 4). At any given time, a maximum of 5 REFab commands can be issued within 1 x tREFI1 window. Self-refresh mode may be entered with a maximum of 4 Refresh commands being postponed. After exiting Self-Refresh mode with one or more Refresh commands postponed, additional Refresh commands may be postponed to the extent that the total number of postponed Refresh commands (before and after the Self-Refresh) will never exceed 4. Self-refresh mode may also be entered with a maximum of 4 Refresh commands pulled in. During Self-Refresh Mode, the number of postponed or pulled in REF commands does not change.

In FGR Mode, the maximum Refresh commands that may be pulled in and postponed is 8, with the resulting maximum interval between the surrounding Refresh commands being limited to 9 x tREFI2 (see Figure 5 and Figure 6). At any given time, a maximum of 9 REFab commands can be issued within 1 x tREFI2 window. The same maximum count of 8 applies to pulled in and postponed Refresh commands around self-refresh entry and exit.

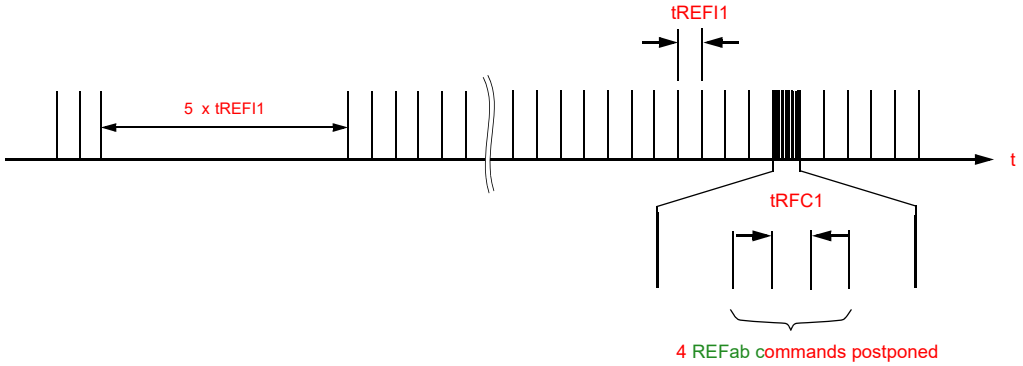


Figure 17 — Postponing Refresh Commands (Example of Normal Refresh Mode - tRFC1)

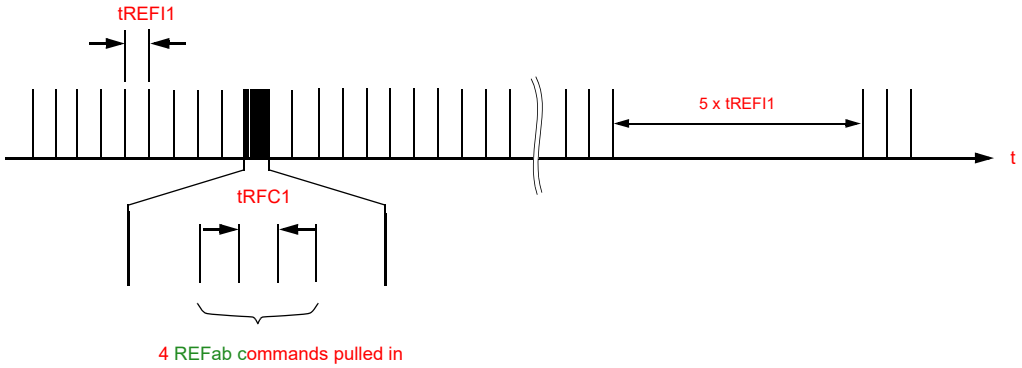


Figure 18 — Pulling in Refresh Commands (Example of Normal Refresh Mode - tRFC1)

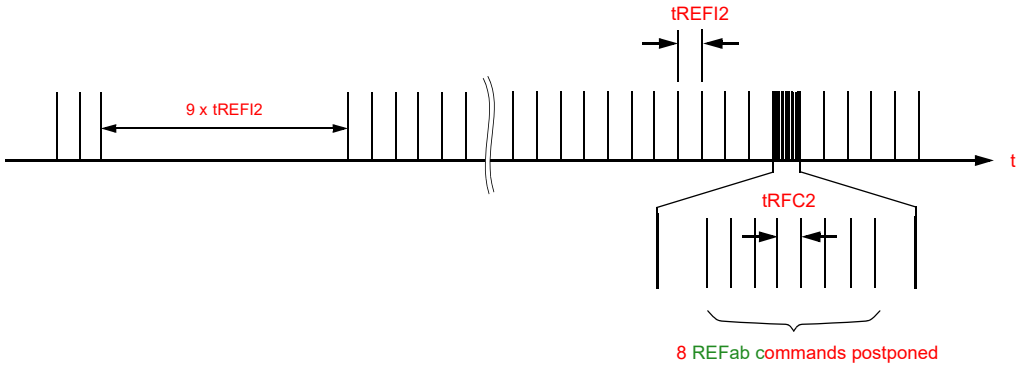


Figure 19 — Postponing Refresh Commands (Example of Fine Granularity Refresh Mode - tRFC2)

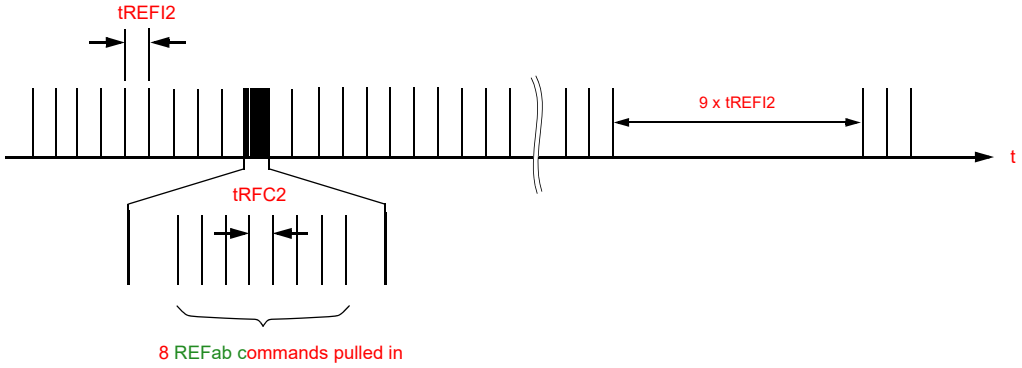


Figure 20 — Pulling in Refresh Commands (Example of Fine Granularity Refresh Mode - tRFC2)

4.10.6 Usage with Temperature Controlled Refresh mode

If the Temperature Controlled Refresh mode is enabled, then only the normal mode is allowed. If FGR mode is selected, then the temperature controlled Refresh mode must be disabled.

4.10.7 Self Refresh entry and exit

DDR5 SDRAM can enter Self Refresh mode anytime in Normal Refresh and FGR mode without any restriction on the number of Refresh commands that have been issued during the mode before the Self Refresh entry. However, upon Self Refresh exit, extra Refresh command(s) may be required depending on the condition of the Self Refresh entry. The conditions and requirements for the extra Refresh command(s) are defined as follows:

1. There are no special restrictions for the Normal Refresh mode.
2. In FGR mode, it is recommended that there should be an even number of REFab commands before entry into Self Refresh since the last Self Refresh exit or MRW command that set the FGR mode. If this condition is met, no additional refresh commands are required upon Self Refresh exit. If this condition is not met, one extra REFab command is required to be issued to the DDR5 SDRAM upon Self Refresh exit. These extra Refresh commands are not counted toward the computation of the average refresh interval (tREFI2).

4.11 Multi-Purpose Command (MPC) - Q3'17 Ballot #1845.01B

4.11.1 Introduction

DDR5-SDRAMs use the Multi-Purpose Command (MPC) to issue commands associated with interface initialization, training, and periodic calibration. The MPC command is initiated with CS, and CA[4:0] asserted to the proper state at the rising edge of CK, as defined by the Command Truth Table. The MPC command has eight operands (OP[7:0]) that are decoded to execute specific commands in the SDRAM.

The MPC command uses an encoding that includes the command encoding and the opcode payload in a single clock cycle. This enables the host to extend the setup and hold for the CA signals beyond the single cycle when the chip select asserts. In addition, the MPC command will support multiple cycles of CS_n assertion. The multiple cycles of CS_n assertion ensures the DRAM will capture the MPC command during at least one rising CK_t/CK_c edge.

Table 27 — MPC Command Definition

Function	Abbreviation	CS	CA Pins														NOTES
			CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13	
Multi Purpose Command	MPC	L	H	H	H	H	L	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	V	

4.11.2 MPC Opcodes

The following table specifies the opcode assignments for the MPC operations:

Table 63 - MPC Command Definition for OP[7:0]

Function	Operand	Data	Notes
Initialization and Training Modes	OP[7:0]	$0000\ 0000_B$: Exit CS Training Mode $0000\ 0001_B$: Enter CS Training Mode $0000\ 0010_B$: RFU $0000\ 0011_B$: Enter CA Training Mode $0000\ 0100_B$: ZQCal Latch $0000\ 0101_B$: ZQCal Start $0000\ 0110_B$: Stop DQS Osc $0000\ 0111_B$: Start DQS Osc $0000\ 1000_B$: Set 2N Command Timing $0000\ 1001_B$: Set 1N Command Timing $0000\ 1010_B$: Exit PDA Enumerate Programming Mode $0000\ 1011_B$: Enter PDA Enumerate Programming Mode $0000\ 11xx_B$: RFU $0001\ 1111_B$: Apply VrefCA and RTT_CA/CS/CK $0010\ 0xxx_B$: Set RTT_CA = xxx $0010\ 1xxx_B$: Set RTT_CS = xxx $0011\ 0xxx_B$: Set RTT_CK = xxx $0011\ 1xxx_B$: Set RTT_PARK = xxx $0100\ xxxx_B$: PDA Enumerate ID = xxxx $0101\ xxxx_B$: PDA Select ID = xxxx All Others: Reserved	1,2,3, 4,5,6,7 ,8, 9

Notes:

1. See command truth table for more information.
2. Refer to the CS Training Mode section for more information regarding CS Training Mode Entry and Exit.
3. Refer to the CA Training Mode section for more information regarding CA Training Mode Entry.
4. Refer to the ZQ Calibration section for more information regarding ZQCal Start and ZQCal Latch.
5. Refer to the DQS Interval Oscillator section for more information regarding Start DQS Osc and Stop DQS Osc
6. Refer to the Per DRAM Addressability section for more information regarding Enter PDA Mode and Exit PDA Mode.

7. Refer to TBD section for more information regarding Set RTT_CA, Set RTT_CS, and Set RTT_CK.
8. “Apply VrefCA and RTT_CA/CS/CK” applies the settings previously sent with the VrefCA command and “MPC Set RTT_CA/CS/CK”. Until this “MPC Apply VrefCA and RTT_CA/CS/CK” command is sent, the values are in a shadow register. Any MRR to the VrefCA and RTT_CA/CS/CK settings should return only the applied value. The shadow register shall retain the previously set value, so that any time the “MPC Apply VrefCA and RTT_CA/CS/CK” command is sent, there is no change in the applied value unless a new VrefCA or RTT_CA/CS/CK value was sent to the shadow register since the previous “MPC Apply VrefCA and RTT_CA/CS/CK” command.
9. The PDA Enumerate ID and PDA Select ID opcodes include a 4-bit value, designated by xxxxB in the table. This is the value that is programmed into the MR for these fields. The PDA Enumerate ID can only be changed while in PDA Enumerate Programming Mode.

4.11.3 MPC Command Timings

As shown in the following figure, the MPC CMD timings can be extended to any number of cycles. The CS_n can also be asserted many consecutive cycles, limited by tMCP_CS. All timings will be relative to the final rising CK_t/CK_c within the CS_n assertion window. The min delay from when the MPC command is captured to the next valid command is specified as tMPC_Delay. Prior to CS Training, the CA will be driven with additional setup and hold beyond the CS_n assertion. Since the alignment between the CS and CK is unknown, the CA setup time tIS will be relative to the CS assertion edge and the CA hold time tIH will be relative to the CS deassertion. The use of the CS assertion and deassertion edges to define the tIS and tIH reference points only applies when the CS is asserted for multiple cycles during the MPC command, which is prior to the completion of CS and CA Training and when the CS Assertion Duration is set to 0 (see below).

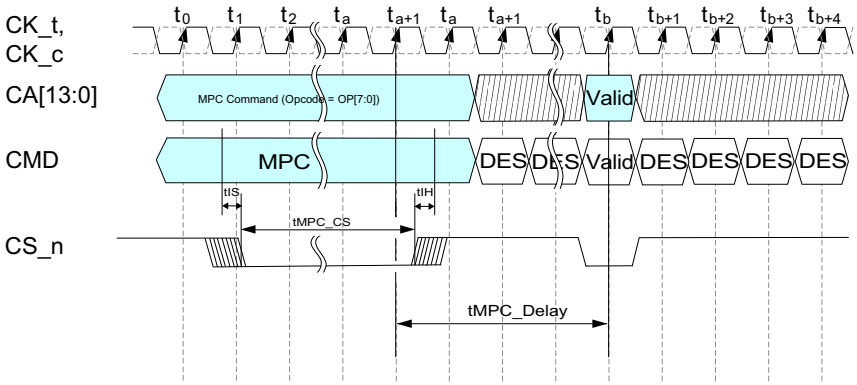


Figure 21 — MPC Command Timing

The DDR5 DRAM will support a MR setting to indicate when a multi-cycle CS assertion may be used for the MPC and VrefCA commands.

Table 28 — MPC and VrefCA CS Assertion Duration

MR Address	Operating Mode	Description
MR3:OP[2]	CS Assertion Duration	**0_B:** Multiple cycles of CS assertion supported for MPC and VrefCA commands **1_B:** Only a single cycle of CS assertion supported for MPC and VrefCA commands

Default value for the CS Assertion Duration is 0, which allows for multi-cycle CS assertions during training. The DRAM shall support going in and out of this mode many times during the DRAM initialization and training sequence. The following timings apply for the multi-cycle CS assertion operation.

Table 29 — AC parameters for MPC Command

Symbol	Description	Min	Max	Unit	Note
tMPC_Delay	MPC to any other valid command delay	TBD	-	nCK	
tMPC_CS	Time CS_n is held low to register MPC command	3.5	8	nCK	1

1 - The minimum tMPC_CS constraint only applies when the CS Assertion Duration setting is 0. The CS Assertion Duration MR setting must be set to enable single cycle MPC commands. The earliest time to set the CS Assertion Duration MR is after CA training is complete, when MRW commands can be sent to the DRAM.

4.12 Per DRAM Addressability (PDA) - Q3'17 Ballot #1845.15A

DDR5 allows programmability of a given device on a rank. As an example, this feature can be used to program different ODT or Vref values on DRAM devices on a given rank. The Per DRAM Addressability (PDA) applies to MRW, MPC, and VrefCA commands. Some per DRAM settings will be required prior to any training of the CA and CS timings and the DQ write timings. The MPC and VrefCA command timings with extended setup/hold and multi-cycle CS assertion may be used for PDA commands if the CA and CS timings have not yet been trained.

DDR5 introduces a CA interface-only method for Per DRAM Addressability, by having a unique PDA Enumerate ID in each DRAM, and the ability to set a PDA Select ID in all DRAM's. The unique PDA Enumerate ID requires the use of the DQ signals and a PDA Enumerate Programming Mode in the DRAM to program. Once the PDA Enumerate ID has been programmed, subsequent commands must not use the DQ signals (Legacy PDA mode) to designate which DRAM is selected for the command. The PDA Enumerate ID is a 4-bit field, and the PDA Select ID is also a 4-bit field. When the PDA Select ID is the same as the PDA Enumerate ID or when the PDA Select ID is set to the "All DRAM" code of 1111_B, the DRAM will apply the MPC, MRW, or VrefCA command. There are a few MPC commands that do not use the PDA Select ID to determine if the command will be applied. Among these MPC commands that do not use the PDA Select ID are the MPC opcodes to set the PDA Enumerate ID and the opcode to set the PDA Select ID. During RESET procedure, the receive FIFO must be initialized with all ones in order to ensure that the PDA enumerate flow does not program an enumerate ID when the strobes are not officially toggling. The table summarizing which MPC commands are dependent on the PDA Select ID values is included below:

Table 30 — Commands that support or don't support PDA Select ID Usage

Command	Opcode	Uses PDA Select ID to determine when to execute command	NOTE
MRW	All	Yes	
VrefCA	All	Yes	
MPC	Set RTT_CA	Yes	
MPC	Set RTT_CS	Yes	
MPC	Set RTT_CK	Yes	
MPC	Set RTT_PARK	Yes	
MPC	Apply VrefCA and RTT_CA/CS/CK	No	
MPC	Enter PDA Enumerate Programming Mode	No	
MPC	Exit PDA Enumerate Programming Mode	No	
MPC	PDA Enumerate ID	No	1
MPC	PDA Select ID	No	
MPC	All other MPC opcodes	No	

Note 1: The PDA Enumerate ID is the only command that utilizes the PDA Enumerate ID Programming mode.

The following mode register fields are associated with Per DRAM Addressable operation:

Table 31 — PDA Mode Register Fields

MR Address	Operating Mode	Description
MR1:OP[3:0]	PDA Enumerate ID[3:0]	This is a **Read Only** MR field, which is only programmed through an MPC command with the PDA Enumerate ID opcode. $xxxx_B$ Encoding is set with MPC command with the PDA Enumerate ID opcode. This can only be set when PDA Enumerate Programming Mode is enabled and the associated DRAM's DQ0 is asserted LOW. The PDA Enumerate ID opcode includes 4 bits for this encoding. Default setting is 1111_B
MR1:OP[7:4]	PDA Select ID[3:0]	This is a **Read Only** MR field, which is only programmed through an MPC command with the PDA Select ID opcode. $xxxx_B$ Encoding is set with MPC command with the PDA Select ID opcode. The PDA Select ID opcode includes 4 bits for this encoding. 1111_B = all DRAM's execute MRW, MPC, and VrefCA commands For all other encodings, DRAM's execute MRW, MPC, and VrefCA commands only if PDA Select ID[3:0] = PDA Enumerate ID[3:0], with some exceptions for specific MPC commands that execute regardless of PDA Select ID. Default setting is 1111_B

4.12.1 PDA Enumerate ID Programming

1. PDA Enumerate Programming Mode is enabled by sending one or more MPC command cycles with TBD opcode.
2. In the PDA Enumerate Programming Mode, only the MPC command with PDA Enumerate ID opcodes is qualified with DQ0 for x4 and x8, and DQL0 for x16. The DRAM captures DQ0 for x4 and x8, and DQL0 for x16 by using DQS_c and DQS_t for x4 and x8, DQSL_c and DQSL_t for x16 signals as shown Figure TBD. If the value on DQ0 for x4 and x8, or DQL0 for x16 is 0 then the DRAM executes the MPC command to set the PDA Enumerate ID. If the value on DQ0 is 1, then the DRAM ignores the MPC command. The controller may choose to drive all the DQ bits. Only the MPC command with PDA Enumerate ID opcodes will be supported in PDA Enumerate Programming Mode, and the MPC command to exit PDA Enumerate Programming Mode does not require a DQ qualification.
3. A complete BL16 set of strobe edges (8 rising edges and 8 falling edges) must be sent by the host within the tPDA_DQS_DELAY min/max range after the MPC command. The DQ value is captured during the last 4 strobe edges. If the DRAM captures a 0 on DQ0 (or DQL0 for x16 devices) at any of the last 4 strobe edges in the strobe sequence, the PDA Enumerate ID command shall be executed by the DRAM**.** Since the write timings for the DQ bus have not been trained, the host must ensure a minimum of 16 strobe edges occurs after a period of tPDA_DQS_Delay(min) after the associated MPC command. The time when the DRAM shall latch the DQ assertion value is tPDA_LATCH. This delay accounts for the latest timing of the DQ assertion from the host and is based on tPDA_DQS_DELAY(max). The BC8 mode register setting in the DRAM is ignored while in PDA Enumerate Programming mode.
4. Prior to when the MPC command for PDA Enumerate Programming Mode entry is sent by the host, the host must drive DQS_t and DQS_c differentially low, other than when the burst of 16 strobe edges is sent in association with the PDA Enumerate ID MPC command. The host must send preamble and postamble DQS_t/DQS_c toggles during the qualification of the PDA command. Once PDA Enumerate Programming Mode is enabled in the DRAM, the host memory controller shall wait tMPC_Delay to the time the first PDA Enumerate ID MPC command is issued.
6. In the PDA Enumerate Programming Mode, only PDA Enumerate ID MPC commands and Exit PDA Enumerate Programming Mode MPC command are allowed.
7. In the PDA Enumerate Programming Mode, the default (or previously programmed) RTT_PARK value will be applied to the DQ signals.
8. The mode register write command cycle time in PDA mode, tPDA_DELAY, is required to complete the write operation to the PDA Enumerate ID mode register and is the minimum time required after the DQ assertion is latched (after tPDA_LATCH), prior to the

next PDA Enumerate ID MPC command as shown in Figure TBD.

9. To remove the DRAM from PDA Enumerate Programming Mode, send an MPC command with opcode encoding [0100:1111], where PDA Enumerate ID = 1111. The Exit PDA Enumerate Programming Mode MPC command is never qualified by the DQ settings and is applied to all DRAMs in the rank.

As an example, the following sequence to program the PDA Enumerate ID per device is as follows:

1. Send MPC with 'Enter PDA Enumerate Programming Mode' opcode
2. For (i = 0, i < MAX_DRAMS, i++)
    a. Send PDA Enumerate ID with i in the opcode (4-bit value), with device i's DQ signals low
3. Send MPC with 'Exit PDA Enumerate Programming Mode' opcode

The following figure shows a timing diagram for setting the PDA Enumerate ID value for one device. In this case only one device is programmed prior to exiting PDA Enumerate Programming Mode, but many devices may be programmed prior to exiting PDA Enumerate Programming Mode.

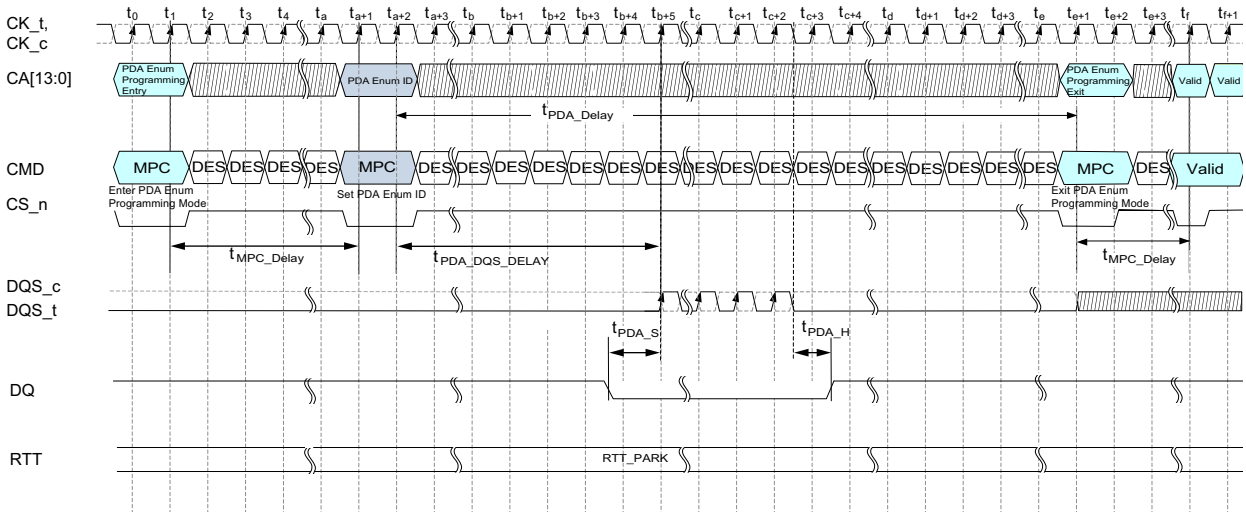


Figure 22 — Timing Diagram showing PDA Enumerate Programming Mode Entry, Programming of PDA Enumerate ID, and PDA Enumerate Programming Mode Exit

***Note** 1- The diagram above assumes preamble/postamble requirements for DQS.*

***Note** 2- The 2nd MPC command at tA+1 is assuming a multi-cycle command and the timings are adjusted to visually show separation between spacing timings such as tMPC_Delay (which start at the end of a command cycle and end at the beginning of the next) and other timings such as tPDA_LATCH.*

4.12.2 PDA Select ID Operation

Once the PDA Enumerate ID's have been programmed in all the DRAM's, the execution of future MPC/MRW/VrefCA commands depend on the value of the PDA Select ID and the type of MPC command. If the PDA Select ID is set to 1111_B, all DRAM's will execute the command. For all MRW commands and VrefCA commands, and some of the MPC commands (RTT_CA/CS/CK and RTT_PARK opcodes), the PDA Select ID will be compared to the PDA Enumerate ID to determine if the DRAM will execute the commands. For all other MPC commands (i.e. not the RTT_CA/CS/CK and RTT_PARK opcodes), the DRAM will execute the command regardless of the PDA Select ID value.

As an example, the following sequence could be used to program unique MR fields per device:

1. Send MPC with 'PDA Select ID' opcode, with encoding 0000 included in the opcode
2. Send MRW's for field settings specific to Device 0000. this can be any number of MRW's
3. Send MPC with 'PDA Select ID' opcode, with encoding 0001 included in the opcode
4. Send MRW's for field settings specific to Device 0001. this can be any number of MRW's
5. Repeat for any number of devices
6. Send MPC with 'PDA Select ID' opcode, with encoding 1111 included in the opcode to enable all DRAM's to execute all MRW, VrefCA, and MPC commands.

The following timing diagram shows an example sequencing of the programming of the PDA Select ID and MPC, VrefCA, or MRW commands.

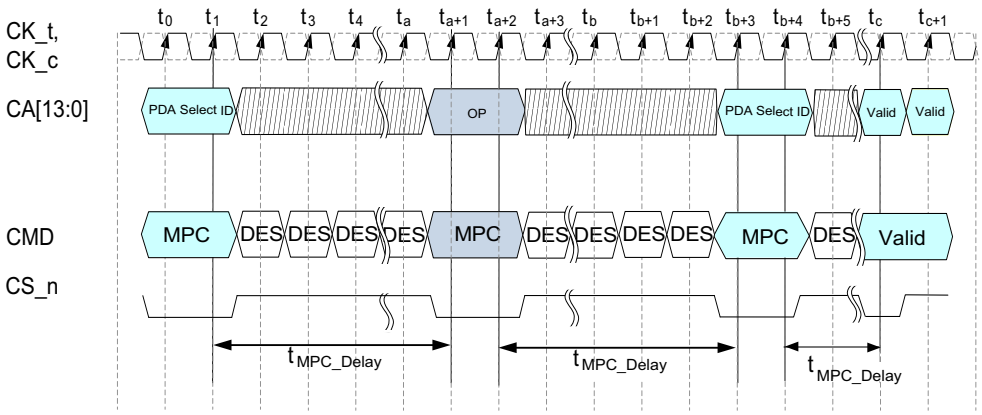


Figure 23 — Timing Diagram showing MPC command sequencing with PDA Select ID

The following table summarizes the electrical parameters associated with PDA Enumerate Programming Mode:

Parameter	Symbol	DDR5-3200 to 4800		DDR5-5200 to 6400		Units	NOTE
		Min	Max	Min	Max		
Delay from PDA command to when the DRAM can latch the DQ assertion feedback	tPDA_LATCH	TBD	TBD	TBD	TBD	nCK	2
Delay from tPDA_LATCH to any other command	tPDA_DELAY	TBD	-	TBD	-	nCK	
Delay to rising strobe edge used for sampling DQ during PDA operation	tPDA_DQS_DELAY	TBD	TBD	TBD	TBD	TBD	1
DQ Setup Time during PDA operation	tPDA_S	TBD	-	TBD	-	TBD	
DQ Hold Time during PDA operation	tPDA_H	TBD	-	TBD	-	TBD	

Note 1: The range of tPDA_DQS_DELAY specifies the full range of when the minimum of 16 strobe edges can be sent by the host controller.

Note 2: This is a worst case cycle delay that indicates the latest time the strobe burst will be completed for the DQ assertion. This value may be an equation based on tPDA_DQS_DELAY.

4.13 Read Training Pattern - Q2'17 Ballot #1845.09A

4.13.1 Introduction

Training of the Memory Interface requires the ability to read a known pattern from the DRAM, prior to enabling writes into the DRAM. Due to the increased frequencies supported by DDR5, a simple repeating pattern will not be sufficient for read training. An LFSR pattern generator will also be required. The read training pattern is accessed when the **host issues an MRR command to a specific MR31 address**. In this case the returned data will be a pattern, instead of the contents of a mode register. The timing of the read data return is the same as for an MRR or Read command, including the operation of the strobes (DQSL_t, DQSL_c, DQSU_t, DQSU_c). The DRAM shall also support non-target ODT. The Read Training Pattern has 2 primary supported modes of operation. One of the modes is referred to as the serial format. The second mode is LFSR mode. The LFSR mode is required due to the higher frequency bus operation for DDR5. There is a secondary mode associated with the LFSR mode, which enables the generation of a simple high frequency clock pattern instead of the LFSR pattern. The Read Training Pattern is a full BL16 pattern for each MRR command issued to the Read Training Pattern address.

Only BL16 Mode is supported by the Read Training Pattern.

Table 32 — Read Training Pattern Address

MR Address	Operating Mode	Description
MR31	Read Training Pattern	This MR address is reserved. There are no specific register fields associated with this address. In response to the MRR to this address the DRAM will send the BL16 read training pattern. All 8 bits associated with this MR address are reserved.

The following table shows the MR field and encodings for the Read Training Pattern format settings.

Table 33 — Read Training Pattern Format

MR Address	Operating Mode	Description	
MR25 OP[0]	Read Training Pattern Format	0 = Serial	1 = LFSR
MR25 OP[1]	LFSR0 Pattern Option	0 = LFSR	1 = Clock
MR25 OP[2]	LFSR1 Pattern Option	0 = LFSR	1 = Clock

The default value for the **Read Training Pattern Format** register setting is: 0x0.

For Serial Read Training Pattern Format mode, the following Mode Registers are programmed with the data pattern. There are two 8-bit registers to provide a 16 UI pattern length and two 8-bit registers to provide up to x16 data width for per-DQ-lane inversion.

Table 34 — Read Pattern Data0 / LFSR0

MR Address	MRW OP	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR26	UI	7	6	5	4	3	2	1	0

The default value for the **Read Pattern Data0/LFSR0** register setting is: 0x5A.

Table 35 — Read Pattern Data1 / LFSR1

MR Address	MRW OP	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR27	UI	15	14	13	12	11	10	9	8

The default value for the **Read Pattern Data1/LFSR1** register setting is: 0x3C.

The values for the **Read Pattern Data0/LFSR0** and **Read Pattern Data1/LFSR1** registers are restored to the default values under the following conditions:

- Power-up initialization
- RESET_n assertion
- Self Refresh
- Power-down entry

The LFSR mode requires an 8-bit Mode Register to program the seed for the 8-bit LFSR. The details of the LFSR polynomial and outputs are explained in the following section. The **Read Pattern Data0/LFSR0** and **Read Pattern Data1/LFSR1** registers are re-purposed to program the LFSR seed when the **Read Training Pattern Format** is set to LFSR.

In both cases, when the **Read Training Pattern Format** is set to Serial mode or LFSR mode, the **Read Pattern Invert - Lower DQ**

Bits and **Read Pattern Invert - Upper DQ Bits** settings will additionally invert the pattern, per DQ bit. The **Read Pattern Invert - Lower DQ Bits** register will apply to x4, x8, and x16 devices. The **Read Pattern Invert - Upper DQ Bits** register only applies to x16 devices, for the upper byte.

Table 36 — Read Pattern Invert - Lower DQ Bits

MR Address	MRW OP	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR28	DQ Invert	DQL7	DQL6	DQL5	DQL4	DQL3	DQL2	DQL1	DQL0

The default value for the **Read Pattern Invert - Lower DQ Bits**register setting is: 0x00.

Table 37 — Read Pattern Invert - Upper DQ Bits

MR Address	MRW OP	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR29	DQ Invert	DQU7	DQU6	DQU5	DQU4	DQU3	DQU2	DQU1	DQU0

The default value for the **Read Pattern Invert - Upper DQ Bits** register setting is: 0x00.

The values for both **Read Pattern Invert - Lower and Upper DQ Bit** registers are restored to the default values under the following conditions:

- Power-up initialization
- RESET_n assertion
- Self Refresh
- Power-down entry

A value of 0 in any bit location of the **Read Pattern Invert - Lower DQ Bits** or **Read Pattern Invert - Upper DQ Bits** registers will leave the pattern un-inverted for the associated DQ. A value of 1 in any bit location of the **Read Pattern Invert - Lower DQ Bits** or **Read Pattern Invert - Upper DQ Bits** registers will invert the pattern for the associated DQ.

4.13.2 LFSR Pattern Generation

The LFSR is an 8-bit Galois LFSR. The polynomial for the Galois LFSR is $x^8+x^6+x^5+x^4+1$. The figure below shows the logic to implement the LFSR. The numbered locations within the shift register show the mapping of the seed/state positions within the register. There are two instances of the same LFSR polynomial. These two instances will have unique seeds/states and supply patterns to any of the DQ outputs.

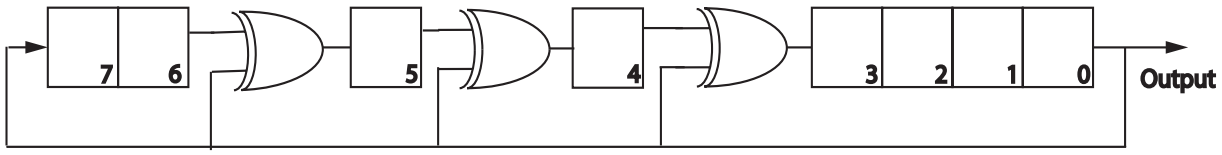


Figure 24 — Read Training Pattern LFSR

The seed location in the figure clarifies the mapping for the **Read Pattern Data0/LFRS0** and **Read Pattern Data1/LFSR1** mode registers relative to the LFSR logic. The LFSR output is directed to any number of the DQ outputs, depending on the LFSR assignment programming. These assignments between LFSR0 and LFSR1 to each DQ output will create a unique pattern sequence for better coverage of DQ to DQ crosstalk interactions. The LFSR assignments are programmed according to the following table:

Table 38 — Read LFSR Assignments

MR Address	MRW OP	LFSR Assignment	MR Setting	
MR30	OP0	DQL0/DQU0	0 = LFSR0	1 = LFSR1
	OP1	DQL1/DQU1	0 = LFSR0	1 = LFSR1
	OP2	DQL2/DQU2	0 = LFSR0	1 = LFSR1
	OP3	DQL3/DQU3	0 = LFSR0	1 = LFSR1
	OP4	DQL4/DQU4	0 = LFSR0	1 = LFSR1
	OP5	DQL5/DQU5	0 = LFSR0	1 = LFSR1
	OP6	DQL6/DQU6	0 = LFSR0	1 = LFSR1
	OP7	DQL7/DQU7	0 = LFSR0	1 = LFSR1

The default value for the **Read LFSR Assignments** register setting is: 0xFE.

The values for the **Read LFSR Assignments** register are restored to the default values under the following conditions:

- Power-up initialization
- RESET_n assertion
- Self Refresh
- Power-down entry

The LFSR output will change at the UI frequency, producing a new output value on every UI. The LFSR will only change state to support the read data after the MRR to the specific (MR31) Read Training Pattern address. When there are no MRR accesses to the (MR31) Read Training Pattern address, the LFSR will retain its previous state (from the end of the previous Read Training Pattern MRR access completion). Therefore, the full state space of the LFSR may be traversed through a series of 16 MRR commands, each of which accesses 16 UI's of LFSR output. The BL for the LFSR data will always be BL16. The state of the LFSR can also be changed by sending a new MRW command to reset the LFSR0 and LFSR1 seed mode registers or through the reset conditions listed for those registers. A setting of 0x00 in either of the LFSR seed registers will not produce a pattern with any transitions to 1. When set to this value the LFSR will produce a constant 0 pattern.

When the **LFSR0 Pattern Option** is set to 1, the pattern that is supplied by the DRAM is a high frequency clock pattern, instead of the LFSR. This clock pattern is sent only to the DQ signals that have a setting of 0 in the corresponding DQ Opcode location in the **Read LFSR Assignments register**. The first UI of the pattern will have a value of 0. The second UI will have a value of 1, and this will continue to toggle for each subsequent UI.

When the **LFSR1 Pattern Option** is set to 1, the pattern that is supplied by the DRAM is a high frequency clock pattern, instead of the LFSR. This clock pattern is sent only to the DQ signals that have a setting of 1 in the corresponding DQ Opcode location in the **Read LFSR Assignments register**. The first UI of the pattern will have a value of 0. The second UI will have a value of 1, and this will continue to toggle for each subsequent UI.

The state of the LFSR will not change when an MRR to MR31 occurs if the associated **LFSR Pattern Option** is set to 1 in MR25[1] for LFSR0 or MR25[2] for LFSR1, designating the clock pattern. The state of both LFSR0 and LFSR1 will also not change when an MRR to MR31 occurs if the serial mode is selected by setting MR25[0] = 0. The **Read LFSR Assignments** settings have no impact on whether or not the LFSR state progresses with each MRR to MR31. Only the **Read Training Pattern Format** and **LFSR Pattern Option** settings determine whether the LFSR is actively computing next states.

4.13.3 Read Training Pattern Examples

The following table shows the bit sequence of the Read Training Pattern, for the following programming:
Read Training Pattern Format = 0 (Serial)
LFSR0 Pattern Option = 0 (These are don't cares when in Serial Read Training Pattern Format)
LFSR1 Pattern Option = 0 (These are don't cares when in Serial Read Training Pattern Format)
Read Pattern Data0/LFSR0 = 0x1C
Read Pattern Data1/LFSR1 = 0x59
Read Pattern Invert - Lower DQ Bits = 0x55
Read Pattern Invert - Upper DQ Bits = 0x55

Table 39 — Serial Bit Sequence Example

Pin	Invert	Bit Sequence															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DQL0	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQL1	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQL2	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQL3	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQL4	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQL5	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQL6	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQL7	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQU0	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQU1	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQU2	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQU3	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQU4	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQU5	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQU6	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQU7	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0

The following table shows the bit sequence of the Read Training Pattern, for the following programming:
Read Training Pattern Format = 1 (LFSR)
LFSR0 Pattern Option = 0
LFSR1 Pattern Option = 0
Read Pattern Data0/LFSR0 = 0x5A
Read Pattern Data1/LFSR1 = 0x3C
Read LFSR Assignments = 0xFE
Read Pattern Invert - Lower DQ Bits = 0x00
Read Pattern Invert - Upper DQ Bits = 0xFF

Table 40 — LFSR Bit Sequence Example

Pin	Invert	LFSR	Bit Sequence															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DQL0	0 (No)	0	0	0	1	1	0	0	0	0	0	0	1	1	1	0	1	0
DQL1	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL2	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL3	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL4	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL5	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL6	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL7	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQU0	1 (Yes)	0	1	1	0	0	1	1	1	1	1	1	0	0	0	1	0	1
DQU1	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU2	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU3	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU4	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU5	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU6	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU7	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1

The following table shows the bit sequence of the Read Training Pattern, for the following programming:
Read Training Pattern Format = 1 (LFSR)
LFSR0 Pattern Option = 0
LFSR1 Pattern Option = 1 (Clock Pattern Option)
Read Pattern Data0/LFSR0 = 0x00 (When the LFSR seed is set to 0, this produces a constant 0 pattern)
Read Pattern Data1/LFSR1 = 0x3C (This value is a don't care when LFSR1 Pattern Option = 1)
Read LFSR Assignments = 0x04
Read Pattern Invert - Lower DQ Bits = 0xFB
Read Pattern Invert - Upper DQ Bits = 0xFB

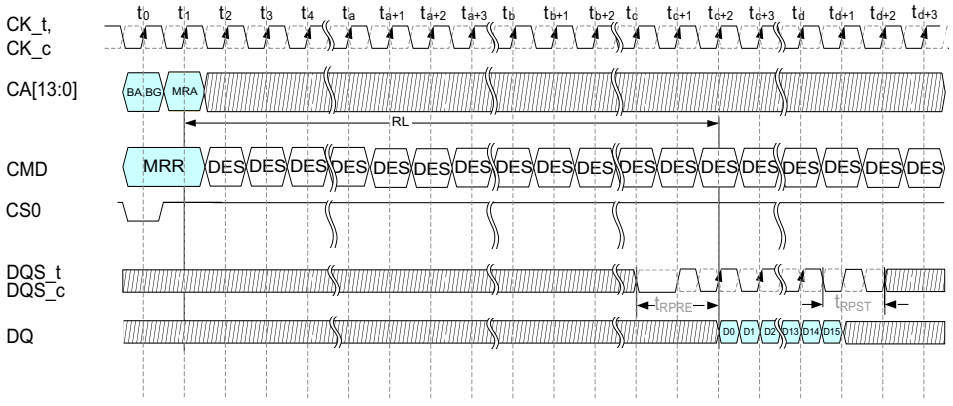
Table 41 — LFSR Bit Sequence Example

Pin	Invert	LFSR	Bit Sequence															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DQL0	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL1	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL2	0 (No)	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
DQL3	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL4	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL5	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL6	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL7	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU0	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU1	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU2	0 (No)	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
DQU3	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU4	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU5	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU6	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU7	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

4.13.4 Read Training Pattern Timing Diagrams

The timing of the data return and strobe sequence should match that of a Read operation. The timing of the Read Training Pattern will be similar to the MRR operation, with the exception that the MRR to the address that invokes the Read Training Pattern will be a full BL16 pattern. The timing between MRR commands to access the Read Training Pattern is defined as tMRR_p, which supports back to back data patterns. This is faster than a normal MRR to MRR condition which is defined as tMRR.

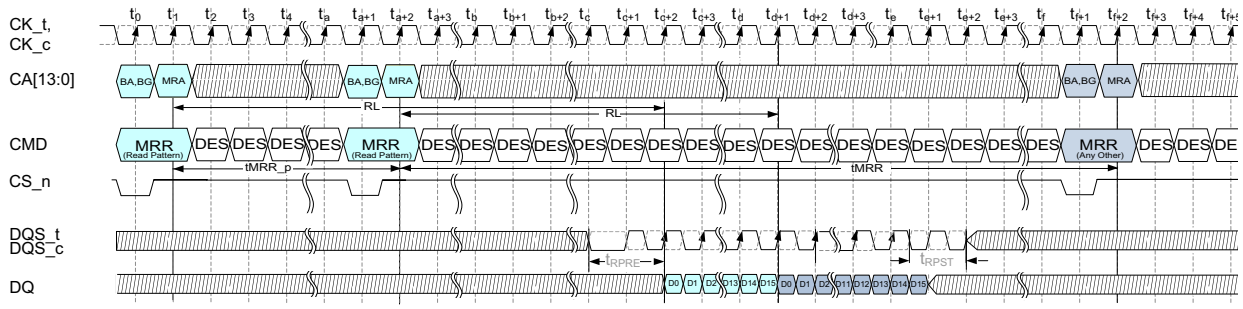
The following timing diagram shows the general timing sequence for an MRR that accesses the Read Training Pattern:



Note - the preamble details are TBD for DDR5. The Read Training Pattern shall align to the DDR5 preamble timings.

Figure 25 — Timing Diagram for Read Training Pattern

The Read Training Pattern must also support back to back traffic, for any number of MRR commands sequenced every 8 tCK. The following timing diagram shows a back to back pattern example:



Note - the preamble details are TBD for DDR5. The Read Training Pattern shall align to the DDR5 preamble timings.

Figure 26 — Timing Diagram for Back to Back Read Training Patterns

Table 42 — AC parameters for Read Training Patterns

Parameter	Symbol	Min/ Max	Data Rate	Unit	Note
Mode Register Read command period	tMRR	Min	16	nCK	
Mode Register Read Pattern to Mode Register Read Pattern Command spacing	tMRR_p	Min	8	nCK	

4.14 Read Preamble Training Mode - Q4'17 Ballot #1845.09 w/Editorial

4.14.1 Introduction

Read preamble training supports read leveling of the host receiver timings. **This mode supports MRR transactions that access the Read Training Pattern**, and cannot be used during any other data transactions. Read preamble training changes the read strobe behavior such that the strobes are always driven by the DRAM, and only toggle during the actual burst of the read data. There is no toggle during the preamble or postamble time. This mode enables the host to detect the timing of when the first data and associated strobe is returned after a read command.

4.14.2 Entry and Exit for Preamble Training Mode

The DRAM is placed into or taken out of Read Preamble Training Mode with the following mode register field.

Table 43 — Read Preamble Training Mode

MR Address	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TBD	Valid	Valid	Valid	Valid	Valid	Valid	Valid	Read Preamble Training Mode

Table 44 — Mode Register Config

Function	Register Type	Operand	Data	Notes
Read Preamble Training Mode Enable	R/W	**OP[0]**	**0_B: Disable** **1_B: Enable (Enter Training Mode)**	

4.14.3 Preamble Training Mode Operation

Once the DRAM is placed in Read Preamble Training Mode, the only data transactions supported are MRR commands. All non-data commands, such as MRW, are still supported in this mode. Once READ Preamble Training is enabled, the device will drive DQS_t LOW and DQS_c HIGH within tSDOn and remain at these levels until an MRR command is issued.

During read preamble training, the DQS preamble provided during normal operation will not be driven by the DRAM. Once the MRR command is issued, the device will drive DQS_t/DQS_c like a normal READ burst after RL. In response to the MRR to the designated Read Training Pattern Address, the device must also drive the DQ pattern as per the Read Pattern configuration while in this mode. The MRR commands may be sequenced to enable back to back bursts on the DQ bus.

Read preamble training mode is exited within tSDOff after setting MR2:OP[0].

The following figure shows the timing for the strobe driven differential low after Read Preamble Training Mode is enabled, and also shows the strobe timings after an MRR command to access the Read Training Pattern:

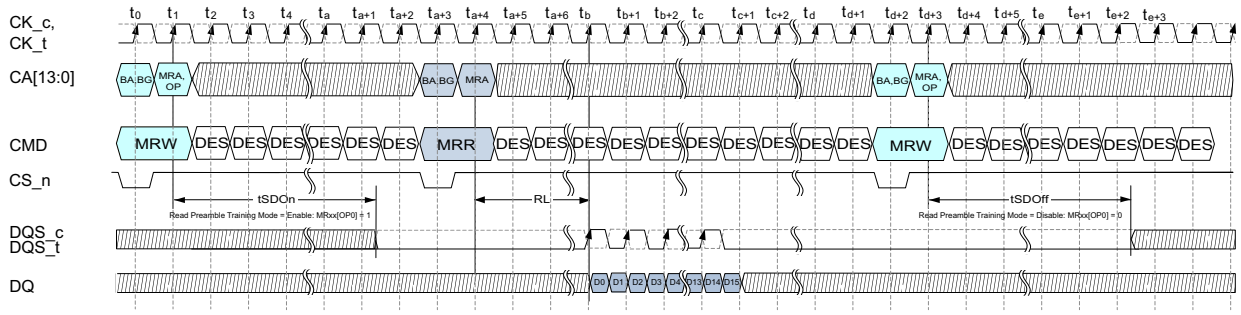


Figure 27 — Timing Diagram for Read Preamble Training Mode Entry, Read Training Pattern Access and Read Preamble Training Mode Exit

Table 45 — Timing parameters for Preamble Training Mode

Parameter	Symbol	Min	Max
Delay from MRW Command to DQS Driven	tSDOn	-	Max(12nCK, 20ns)
Delay from MRW Command to DQS Disabled	tSDOff	-	Max(12nCK, 20ns)

4.15 CA Training Mode (CATM) - Q4'16 Ballot #1845.02

4.15.1 Introduction

The CA Training Mode is a method to facilitate the loopback of a logical combination of the sampled CA[13:0] signals. In this mode, the CK is running, and the CS_n qualifies when the CK samples the CA signals. A loopback equation that includes all the CA signals results in an output value that is sent asynchronously on the DQ signals back to the host memory controller. The host timings between CS_n, CK, and CA[13:0] signals can then be optimized for proper alignment. When the DRAM is in this mode, no functional commands are executed in the DRAM. The functional command interface is restored only after exiting this mode, which requires a CS_n assertion of two or more consecutive tCK.

4.15.2 Entry and Exit for CA Training Mode

The CA Training Mode is enabled through an MPC command, with the opcode designated for CA Training Mode Entry**.** Once this MPC command has executed no other commands will be interpreted by the DRAM. Only the sampling of the CA signals, evaluation of the XOR result, and loop back to the DQ's will occur. While in CA Training Mode, the CS_n signal will only assert for a single tCK at a time. The maximum sampling rate on the CA signals will be every 4tCK.

The CA Training Mode is disabled by asserting CS_n for 2 or more cycles in a row, while sending a NOP command on the CA bus.

4.15.3 CA Training Mode (CATM) Operation

In CA Training Mode, the CA values are sampled in the same way as for functional operation, where the CS_n qualifies which cycle the sampling occurs, and the sample is captured by the rising CK edge. Unlike functional operation, there is no concept of multiple cycle commands in CA Training Mode. Sampling of the CA signals ONLY occurs when CS_n is asserted. Once the CA signals are sampled, the values are XOR'd to produce an output value. This output value is driven on all the DQ pins, as a pseudo-static value. These output values will be held until the next sample is captured on the CA bus, according to the CS_n assertion.

During CA Training Mode the CA ODT is enabled as for functional operation. The VrefCA is set according to the functional setting (through the VrefCA Command). The timing requirements for the CA bus, CK_t, CK_c, and CS_n are the same as for functional operation.

The delay from when the CA signals are sampled during the CS_n assertion and when the output of the XOR computation is driven on the DQ pins is specified as t_{CATM_Valid}, as shown in the following figure. CS_n shall be asserted every 4tCK or with greater than 4tCK separation between assertions, and thus the CA XOR output shall transition every 4tCK or greater. The following figure demonstrates an example where two CS_n assertions occur with a separation of 4tCK. The DRAM will exit CA Training Mode when the CS_n is asserted for 2 or more consecutive cycles but limited to TBD.

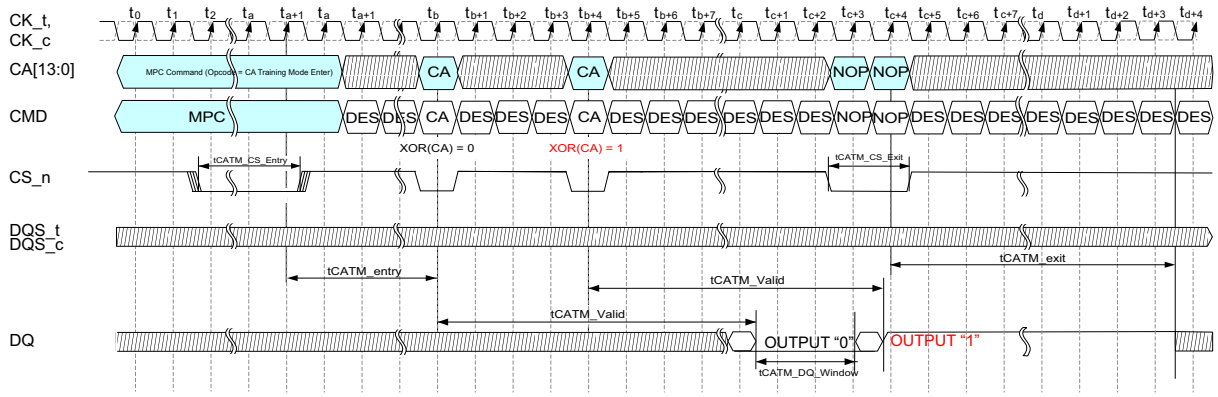


Figure 28 — Timing Diagram for CA Training Mode

Table 46 — AC parameters for CA Training Mode

Symbol	Min	Max	Unit
tCATM_Entry	-	20	ns
tCATM_Exit	-	20	ns
tCATM_Valid	-	20ns	ns
tCATM_DQ_Window	2	-	nCK
tCATM_CS_Entry	TBD	8	nCK
tCATM_CS_Exit	2	8	nCK

4.15.3.1 CA Loopback Equations

The CATM Output is computed based on the CS_n assertion and the values of the CA inputs. The following table clarifies the output computation.

Table 47 — CA Training Mode Output

CS_n	CATM Output
0	XOR(CA[13:0])[1]
1	Hold previous value

1. The XOR function occurs after mirroring/inversion recovery, and only includes signals supported on the DRAM (i.e. may not include up to CA[13], depending on density.) For any CA signals not supported in the DRAM, the logical value of these signals shall be considered 0 for the XOR computation.

4.15.3.2 Output equations

The following table shows which signals will transmit the output of the CA Training Mode loopback equation. These values are driven asynchronously as pseudo-static values, updating with a new output at a time t_{CATM_Valid} after each CS_n assertion.

Table 48 — Output Equations per Interface Width

Output	X16	X8	X4
DQ0	CATM Output	CATM Output	CATM Output
DQ1	CATM Output	CATM Output	CATM Output
DQ2	CATM Output	CATM Output	CATM Output
DQ3	CATM Output	CATM Output	CATM Output
DQ4	CATM Output	CATM Output	
DQ5	CATM Output	CATM Output	
DQ6	CATM Output	CATM Output	
DQ7	CATM Output	CATM Output	
DML			
TDQS_c			
DQSL			
DQSL_B			
DQ8	CATM Output		
DQ9	CATM Output		
DQ10	CATM Output		
DQ11	CATM Output		
DQ12	CATM Output		
DQ13	CATM Output		
DQ14	CATM Output		
DQ15	CATM Output		
DMU			
DQSU			
DQSU_B			

4.16 CS Training Mode (CSTM) - Q4'16 Ballot #1845.10

4.16.1 Introduction

The CS Training Mode is a method to facilitate the loopback of a sampled sequence of the CS_n signal. In this mode, the CK is running, and the CA signals are held in a NOP command encoding state. Once this mode is enabled and the DRAM devices are selected to actively sample and drive feedback, The DRAM will sample the CS_n signal on the rising edge of CK. Every set of four CK rising edge samples will be included in a logical computation to determine the CSTM Output result that is sent back to the host on the DQ bus. Once sampling begins, the DRAM must maintain the consecutive grouping of the samples every 4 tCK. When the CS_n Sample[0] and Sample[2] results in a logic 0 and the CS_n Sample[1] and Sample[3] results in a logic 1, the DRAM will drive a 0 on all the DQ signals. There is no requirement to drive any strobes, and the output signal could transition as often as every 4 tCK.

4.16.2 Entry and Exit for CS Training Mode

The CS Training Mode is enabled when the host sends an MPC command with the opcode for CS Training Mode Entry. Since CS Training must occur prior to establishing alignment between CK and CS_n signals, the MPC command extends beyond multiple tCK cycles, during which the CS_n signal is asserted. When the DRAM is in this mode, commands are still actively processed. The only commands that should be sent by the host memory controller while CS Training Mode is enabled are the NOP command and the MPC to exit CS Training Mode. Any other command may produce unreliable results. Once the DRAM has CS Training Mode enabled, the DRAM begins sampling on every rising CK edge, with the 4-sample groups looping consecutively. Depending on the value of the samples, the DQ signals are driven high or low. Prior to entering CS Training Mode, the DQ signals are not driven by the DRAM and are terminated according to the default RTT_PARK setting. After CS Training Mode is enabled, the DQ signal will begin driving the output values based on the CS Training Mode samples. Once the DQ signals are driven by the DRAM, RTT_PARK termination will no longer be applied, similar to a READ operation.

To exit CS Training Mode, an MPC command must be sent to disable CS Training Mode. Since the timing relationship between CS_n and CK is understood when exiting CS Training Mode, the host can either send a multi-cycle CS_n assertion during the MPC command or a single tCK assertion.

4.16.3 CS Training Mode (CSTM) Operation

In CS Training Mode, the CS_n values are sampled on all CK rising edges. Each group of 4 consecutive samples is evaluated in pairs, and then the two pairs are combined with a logical OR prior to sending to the DQ output. The samples evaluation to determine the output is as follows:

Table 49 — Sample Evaluation for Intermediate Output[0]

Output[0]	CS_n Sample[0]	CS_n Sample[1]
1	0	0
0	0	1
1	1	0
1	1	1

Table 50 — Sample Evaluation for Intermediate Output[1]

Output[1]	CS_n Sample[2]	CS_n Sample[3]
1	0	0
0	0	1
1	1	0
1	1	1

Table 51 — Sample Evaluation for final CSTM Output

CSTM Output*	Output[0]	Output[1]
0	0	0
1	0	1
1	1	0
1	1	1

*When there is no change on the CSTM Output from previous evaluation, DQ shall continue to drive same value continuously with no switching on the bus.

During CS Training Mode the CA ODT is enabled as for functional operation. The VrefCA is set according to the functional setting (through the VrefCA Command).

The delay from when the CS signals are sampled during the fourth CK rising edge (Sample[3]) to when the output of the sample evaluation is driven to a stable value on the DQ pins is specified as t_{CSTM_Valid}, as shown in the following figure. The details of the tCSTM_entry, tCSTM_exit, and tCSTM_DQ_Window are also illustrated.

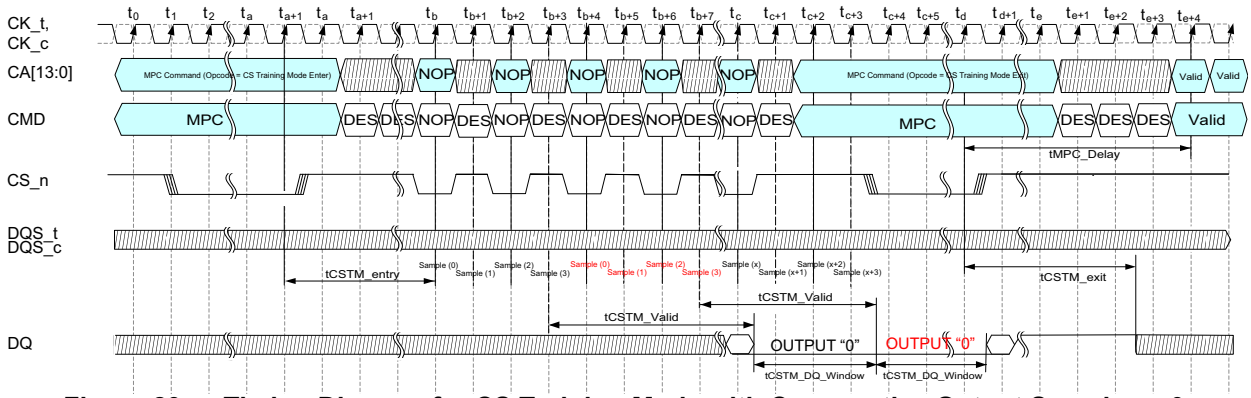


Figure 29 — Timing Diagram for CS Training Mode with Consecutive Output Samples = 0

The following figure illustrates an example where the DQ Output switches from a logic 0 to a logic 1 value, demonstrating the minimum tCSTM_DQ_Window:

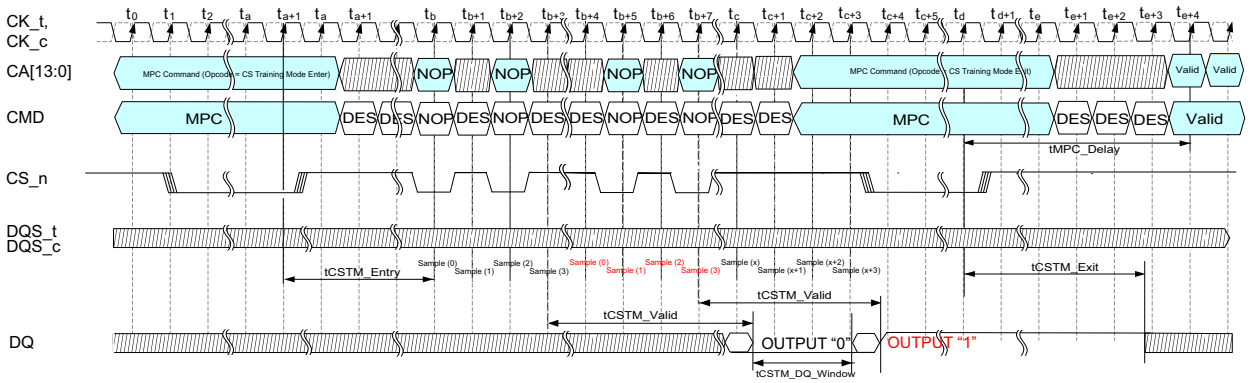


Figure 30 — Timing Diagram for CS Training Mode with Output Sample Toggle

Note 1 - See MPC Command for details on Setup, Hold and command register time.

Table 52 — AC parameters for CS Training Mode

Symbol	Description	Min	Max	Unit	Note
tCSTM_Entry	Registration of CSTM entry command to start of training samples time	-	20	ns	
tCSTM_Exit	Registration of CSTM exit command to end of training mode	-	14	ns	
tCSTM_Valid	Time from sample evaluation to output on DQ bus	-	20	ns	
tCSTM_DQ_Window	Time output is available on DQ Bus	2	-	nCK	
tMPC_Delay	MPC to any other valid command delay	tMRD	-	nCK	
~~tCSTM_CS_Entry~~	~~Time CS_n is held low to register entry command~~	~~3.5~~	~~8~~	~~nCK~~	~~1~~
~~tCSTM_CS_Exit~~	~~Time CS_n is held low to register exit command~~	~~TBD~~	~~8~~	~~nCK~~	~~2~~
~~tCSTM_SU~~	~~Command to CS_n low Setup time~~	~~TBD~~		~~TBD~~	
~~tCSTM_HD~~	~~CS_n high to Command Hold time~~	~~TBD~~		~~TBD~~	

Note:
~~1 - Multiple cycles are used to avoid possible metastability of CS_n.~~
~~2 - At the end of CSTM, it is assumed that the host should be able to place the CS_n appropriately and the exit command could be issued as a single cycle command.~~

4.16.3.1 Output signals

The following table shows which signals will transmit the output of the CS Training Mode loopback sample evaluation. These values are driven asynchronously, but may switch as often as every 4tCK.

Table 53 — CS Sampled Output per Interface Width

Output	X16	X8	X4
DQ0	CSTM Output	CSTM Output	CSTM Output
DQ1	CSTM Output	CSTM Output	CSTM Output
DQ2	CSTM Output	CSTM Output	CSTM Output
DQ3	CSTM Output	CSTM Output	CSTM Output
DQ4	CSTM Output	CSTM Output	
DQ5	CSTM Output	CSTM Output	
DQ6	CSTM Output	CSTM Output	
DQ7	CSTM Output	CSTM Output	
DML			
TDQS_c			
DQSL			
DQSL_B			
DQ8	CSTM Output		
DQ9	CSTM Output		
DQ10	CSTM Output		
DQ11	CSTM Output		
DQ12	CSTM Output		
DQ13	CSTM Output		
DQ14	CSTM Output		
DQ15	CSTM Output		
DMU			
DQSU			
DQSU_B			

4.17 Write Leveling (WL) Training Mode - Q4'16 Ballot #1830.68 w/Editorial Updates

4.17.1 Introduction

The DDR5 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR5 SDRAM supports a 'write leveling' feature to allow the controller to compensate for channel skew.

The memory controller can use the 'write leveling' feature and feedback from the DDR5 DRAM to adjust the DQS_t - DQS_c to align to the phase and cycle that corresponds to the CWL delay after the WRITE command. The memory controller involved in the leveling must have adjustable delay setting on DQS_t - DQS_c to align the rising edge of DQS_t - DQS_c with the timing at the receiver that is the internal DRAM CWL timing point. The internal DRAM CWL timing point may be skewed from the pin-level CWL timing point, but must be within a constrained time window tWL_internal_skew relative to the pin-level CWL timing point. The internal CWL timing point is indicated by an internal WL pulse that begins tWL_ADJ (~0.5 tCK) prior to the internal CWL timing point and extends for ~1tCK.

While in Write Leveling Mode, the DRAM asynchronously feeds back the internal WL pulse, sampled with the rising edge of DQS_t - DQS_c, through the DQ bus. The internal WL pulse is generated in response to a WRITE command. The controller repeatedly delays DQS_t - DQS_c, sends a WRITE command, and monitors the DQ feedback until a transition from 0 to 1 is detected. The host must apply an additional tWL_ADJ (~0.5 tCK) offset to the DQS_t - DQS_c delay to align to the internal CWL timing point. When this is complete, the DQS_t - DQS_c is phase aligned and cycle aligned for write operations. During the training sequence the DRAM in WL training mode will apply ODT to the strobes in the same way as for functional operation. All non-target ranks (which will not be in WL Training Mode) will apply ODT as defined for functional operation.

In addition to the WL Training Mode, there is a WL Init mode. This WL Init mode enables the DRAM to determine internal timing of the enabling of the DRAM receivers based on the WRITE command and the Write Latency setting. If needed, the DRAM may adjust the timing of the internal DRAM receiver enable signal, and thus adjust the internal WL pulse used in WL Training mode.

4.17.2 WL Mode Registers

The MR fields for WL Init and WL Training modes are listed below. To enter each mode, the respective field is set to a 1. To exit the mode, the respective field is set to 0. The WL Init mode and the WL Training mode shall not be enabled simultaneously.

This MR area is subject to move once all of the registers start to get defined.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU						WL Training	WL Init

Function	Register Type	Operand	Data	Notes
WL Init	R/W	**OP[0]**	**0_B: Disable** **1_B: Enable**	**1,2**
WL Training	R/W	**OP[1]**	**0_B: Disable** **1_B: Enable**	**3,4**
RFU	TBD	**OP[7:2]**		

NOTE:
1. To enter WL Init Mode the following MR field must be programmed to 1.
2. To exit WL Init Mode the MR field must be programmed to 0.
3. To enter WL Training Mode the following MR field must be programmed to 1.
4. To exit WL Training Mode the MR field must be programmed to 0.

4.17.3 WL Init Operation

WL Init is a function added to the standard WL mode to give the DRAM the opportunity for coarse alignment of the internal WL pulse ~~to~~ to the DRAM input level of the CK_t, tCK_c with respect to Write Latency.

After the WL init is enabled, a dummy WRITE command is issued by the host. The DRAM will watch for the appropriate DQS that traditionally comes with the WRITE, after the WL (Write Latency). The DQ bus may be quiet or driven.The host controller may send the ACT and PRE associated with the WRITE command or only send the WRITE. The DRAM will ignore the ACT and PRE commands and the address for the ACT and WRITE commands may be any address.

When WL Init is enabled, the host will drive a static state of DQS_t/DQS_c after tWDSO and maintain it until the following WRITE command's DQS toggling starts and will resume driving a static state after the DQS toggle completes. The static state of DQS will be held until tWDSO, following the disabling of WL Init by another MRW command. The DRAM may choose to ignore this function if the internal skew between CK and their internal WL pulse is less than TBD clock(s).

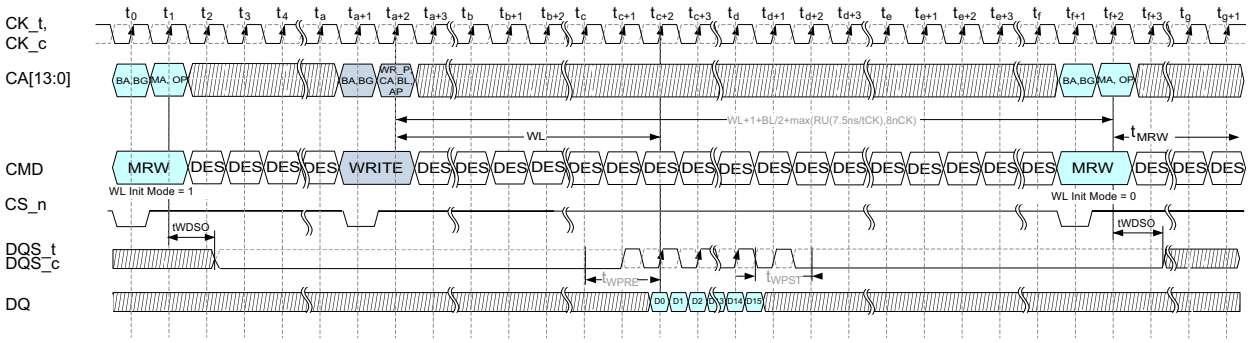


Figure 31 — Timing Diagram for WL Init Mode

4.17.4 WL Training Operation

When WL Mode is enabled, the DRAM will have an internal WL pulse centered on the CWL time after the WRITE command. This is the only cycle where the strobe from the host will sample a non-zero value.

DQS_t - DQS_c driven by the controller during leveling mode must be terminated by the DRAM based on ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

All data bits shall carry the leveling feedback to the controller across the DRAM configurations X4, X8, and X16. On a X16 device, both byte lanes shall be leveled independently. Therefore, a separate feedback mechanism shall be available for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS(diff_UDQS) to internal WL pulse relationship whereas the lower data bits would indicate the lower diff_DQS(diff_LDQS) to internal WL pulse relationship.

The following diagram shows the timing sequence to enter WL Mode, operation during WL Mode, and the timing sequence to exit WL mode. An MRW command is sent to enable WL Mode. After tWLDQSEN time, the controller can send a WR command, followed by strobe pulses. There is no restriction as to when the strobe pulses are sent, so long as they are after the WR command. Each rising edge of DQS_t/DQS_c samples the internal WL pulse and the DRAM sends this sample on all DQ lanes tWLO after the sample.

While in WL Training mode, the host controller may send ACT and PRE commands. The DRAM will ignore these commands. The address associated with the ACT and the WRITE commands may be any value.

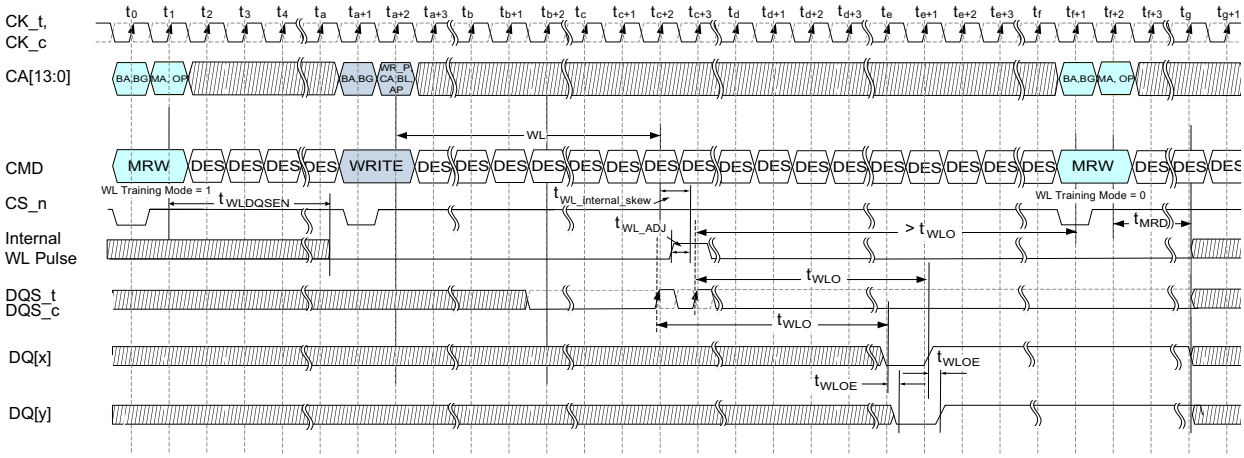


Figure 32 — Timing Diagram for WL Training Mode

The Memory controller initiates Leveling mode of all DRAMs by setting TBD MR field to 1. When entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only WRITE commands and MRW commands are allowed. Since the controller levels one rank at a time, all non-target ranks will set Write Leveling Mode to disabled. The Controller may assert non-target ODT through the normal WRITE command protocol. The target WRITE ODT will apply to the DQS_t and DQS_c signals.

The Controller may drive DQS_t low and DQS_c high any time after the WRITE command. The WRITE command must occur after a delay of tWLDQSEN relative to when the MRW enabled Write Leveling Mode. The controller provides any number of DQS_t, DQS_c edges in the range of a single pulse to a full burst length of strobe pulses. Each rising edge of the strobe is used by the DRAM to sample the internal WL pulse, which asserts 0.5 tCK prior to the internal CWL timing point and remains asserted for ~1tCK duration.

DRAM samples the internal WL pulse with rising edge of DQS_t - DQS_c and provides feedback on all the DQ bits asynchronously after tWLO timing. There is a DQ output uncertainty of tWLOE defined to allow mismatch on DQ bits. The tWLOE period is defined from the transition of the earliest DQ bit to the corresponding transition of the latest DQ bit. There are no read strobes (DQS_t/ DQS_c) needed for these DQs. Controller samples incoming DQ and decides to increment or decrement DQS_t - DQS_c delay setting and launches the next WRITE command with associated DQS_t/DQS_c pulse (or pulse sequence) after some time, which is controller dependent. Once a 0 to 1 transition is detected, the controller locks DQS_t - DQS_c delay setting and write leveling is achieved for the device. If more than one DQS_t/DQS_c pulse was sent by the controller, there is an offset within the controller timings that needs to be applied to account for the timing of the last sample relative to functional timings. There is also a tWL_ADJ (~0.5 tCK) offset to align to the internal CWL timing point relative to when the internal WL pulse asserts.

Parameter	Symbol	DDR5-3200 to 4800		DDR5-5200 to 6400		Units	NOTE
		Min	Max	Min	Max		
DQS_t/DQS_n delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	nCK	
Write leveling output	tWLO	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE	0	2	0	2	ns	
WL internal skew of WL sampling pulse center to CWL CK_t/CK_c edge	tWL_internal_skew	TBD	TBD	TBD	TBD	TBD	
Delta from the rising edge of the internal WL pulse to the internal CWL timing point	tWL_ADJ	TBD	TBD	TBD	TBD	tCK	
Write leveling Init to start driving of DQS static state	tWDSO	TBD	TBD	TBD	TBD	tCK	

4.17.5 DRAM Termination During Write Leveling

When the DRAM is in Write Leveling Mode, the DQS_c/DQS_t termination will be the same as for functional operation. The DQ signals will not be terminated in the DRAM, but instead will be driving values to the controller. The host controller will apply termination for the DQ signals.

ODT Enabled	DQS_t/DQS_c Termination	DQ Termination
RTT_WR	RTT_WR, according to WR Timings	Off
RTT_PARK, RTT_WR disabled	RTT_PARK	Off

4.18 Connectivity Test (CT) Mode - Q4'16 Ballot #1845.06 w/Editorial Updates

4.18.1 Introduction

The DDR5 memory device supports a connectivity test (CT) mode, which is designed to greatly speed up testing of electrical continuity of pin interconnection on the PC boards between the DDR5 memory devices and the memory controller on the SoC. Designed to work seamlessly with any boundary scan devices, the CT mode is required for **all** DRAM devices independent of density and interface width. This applies to x4, x8, and x16 interface widths. Contrary to other conventional shift register based test modes, where test patterns are shifted in and out of the memory devices serially in each clock, DDR5's CT mode allows test patterns to be entered in parallel into the test input pins and the test results extracted in parallel from the test output pins of the DDR5 memory device at the same time, significantly enhancing the speed of the connectivity check.

Prior to entering CT Mode, RESET_n is registered to High. The CT Mode is enabled by asserting the Test Enable (TEN) pin. During CT Mode, the DRAM will set the internal VrefCA to the default VrefCA reset value. The DRAM will set the internal CA ODT to the default CA ODT reset value. It is TBD whether or not the same VrefCA and CA ODT values will apply to the ALERT_n receiver for the CT Mode.

Once put in the CT mode by asserting the TEN pin, the DDR5 memory device effectively appears as an asynchronous device to the external controlling agent; after the input test pattern is applied, the connectivity test results are available for extraction in parallel at the test output pins after a fixed propagation delay. During CT mode, CA ODT is set to the default reset value. A reset of the DDR5 memory device is required after exiting the CT mode.

4.18.2 Pin Mapping

Only digital pins can be tested via the CT mode. For the purpose of connectivity check, all pins that are used for the digital logic in the DDR5 memory device are classified as one of the following types:

1. Test Enable (TEN) pin: when asserted high, this pin causes the DDR5 memory device to enter the CT mode. In this mode, the normal memory function inside the DDR5 memory device is bypassed and the IO pins appear as a set of test input and output pins to the external controlling agent. The DRAM will set the internal VrefCA to the default VrefCA reset value. The DRAM will set the internal CA ODT to the default CA ODT reset value. The TEN pin is dedicated to the connectivity check function and will not be used during normal memory operation.
2. Chip Select (CS_n) pin: when asserted low, this pin enables the test output pins in the DDR5 memory device. When de-asserted, the output pins in the DDR5 memory device will be tri-stated. The CS_n pin in the DDR5 memory device serves as the CS_n pin when in CT mode.
3. Test Input: a group of pins that are used during normal DDR5 DRAM operation are designated as test input pins. These pins are used to enter the test pattern in CT mode. Most Test Input pins are input pins during normal operation. The ALERT_n pin is the only output pin that will be used as a Test Input during CT mode. The CK_t and CK_c pins are single-ended Test Input pins during CT Mode.
4. Test Output: a group of pins that are used during normal DDR5 DRAM operation are designated test output pins. These pins are used for extraction of the connectivity test results in CT mode.
5. Reset: Fixed high level for RESET_n is required during CT mode, same as normal function.

Table 54 below shows the pin classification of the DDR5 memory device.

Table 54 — Pin Classification of DDR5 Memory Device in Connectivity Test(CT) Mode

Pin Type in CT Mode		Pin Names during Normal Memory Operation
Test Enable		TEN
Chip Select		CS_n
Test Inputs	A	CA[13:0]
	B	CK_t, CK_c
	C	ALERT_n
Test Outputs		DQL[7:0], DQU[7:0], DQSU_t, DQSU_c, DQSL_t, DQSL_c, DML_n, DMU_n, DM_n/TDQS_t, TDQS_c
Reset		RESET_n

NOTE: Test Outputs may contain the Upper and Lower label identification used with x16 devices. In the case of x4/x8 devices, the lower (L) identification may be removed.

Table 55 — Signal Description

Symbol	Type	Function
TEN	Input	Connectivity Test Mode is active when TEN is HIGH and inactive when TEN is LOW. TEN must be LOW during normal operation TEN is a CMOS rail-to-rail signal with DC high and low at 80% and 20% of VDD.

4.18.3 Logic Equations

4.18.3.1 Min Term Equations

MTx is an internal signal to be used to generate the signal to drive the output signals. These internal signals are the same across all interface widths and densities.

Table 56 — Min Term Equations

Min Term	Intermediate Logic Nodes
MT0	XOR(CA[0,1,2,3,8,9,10,11])
MT1	XOR(CA[0,4,5,6,8,12,13], ALERT_n)
MT2	XOR(CA[1,4,9,12], CK_t, CK_c)
MT3	XOR(CA[2,5,7,10,13], CK_t)
MT4	XOR(CA[3,6,7,11], CK_c, ALERT_n)
MT0_B	!(MT0)
MT1_B	!(MT1)
MT2_B	!(MT2)
MT3_B	!(MT3)
MT4_B	!(MT4)

4.18.3.2 Output equations

Table 57 — Output Equations per Interface Width

Output	X16	X8	X4
DQL0	MT0	MT0	MT0
DQL1	MT1	MT1	MT1
DQL2	MT2	MT2	MT2
DQL3	MT3	MT3	MT3
DQL4	MT0_B	MT0_B	
DQL5	MT1_B	MT1_B	
DQL6	MT2_B	MT2_B	
DQL7	MT3_B	MT3_B	
DML	MT4	MT4	
TDQS_c		MT4_B	
DQSL_t	MT4	MT4	MT4
DQSL_c	MT4_B	MT4_B	MT4_B
DQU0	MT0		
DQU1	MT1		
DQU2	MT2		
DQU3	MT3		
DQU4	MT0_B		
DQU5	MT1_B		
DQU6	MT2_B		
DQU7	MT3_B		
DMU	MT4		
DQSU_t	MT4		
DQSU_c	MT4_B		

NOTE: Test Outputs may contain the Upper and Lower label identification used with x16 devices. In the case of x4/x8 devices, the lower (L) identification may be removed.

4.18.4 Input level and Timing Requirement

During CT Mode, input levels are defined below.
TEN pin: CMOS rail-to-rail with DC high and low at 80% and 20% of VDDQ.
CS_n: Pseudo differential signal referring to internal VrefCA
Test Input pins : Pseudo differential signal referring to internal VrefCA
RESET_n: CMOS DC high above 70 % VDD

Prior to the assertion of the TEN pin, all voltage supplies must be valid and stable.

Upon the assertion of the TEN pin, the CK_t and CK_c signals will be ignored and the DDR5 memory device will enter into the CT mode after time tCT_Enable. In the CT mode, no refresh activities in the memory arrays, initiated either externally (i.e., auto-refresh) or internally (i.e., self-refresh), will be maintained.

The TEN pin may be asserted after the DRAM has completed power-on, after RESET_n has de-asserted, the wait time after the RESET_n de-assertion has elapsed, and prior to starting clocks (CK_t, CK_c).

The TEN pin may be de-asserted at any time in the CT mode. Upon exiting the CT mode, the states of the DDR5 memory device are unknown and the integrity of the original content of the memory array is not guaranteed; therefore, the reset initialization sequence is required.

All output signals at the test output pins will be stable within tCT_valid after the test inputs have been applied to the test input pins with TEN input and CS_n input maintained High and Low respectively.

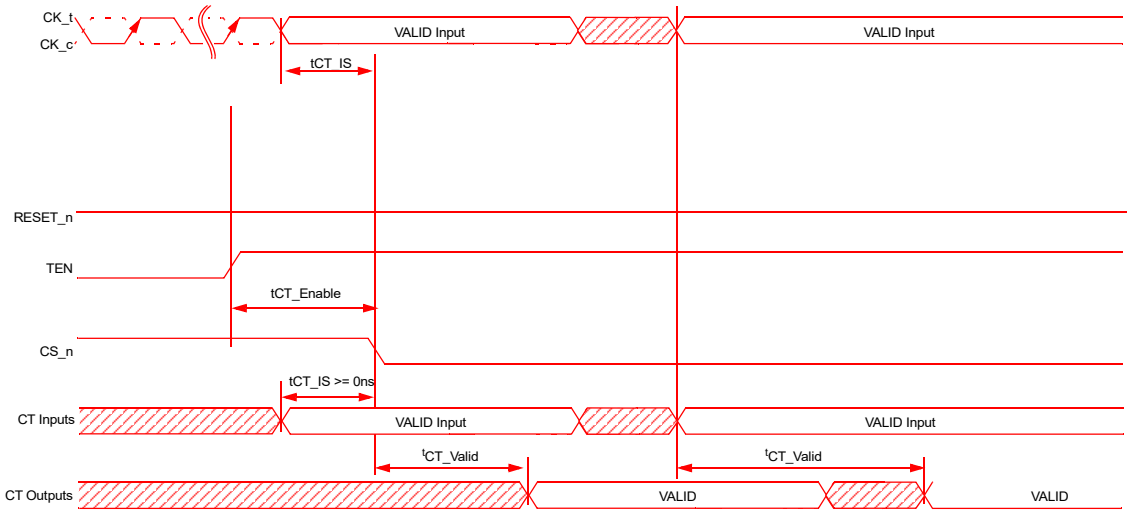


Figure 33 — Timing Diagram for Connectivity Test (CT) Mode

Table 58 — AC parameters for Connectivity Test (CT) Mode

Symbol	Min	Max	Unit
tCT_IS	0	-	ns
tCT_Enable	200	-	ns
tCT_Valid	-	200	ns

4.18.5 Connectivity Test (CT) Mode Input Levels

Following input parameters will be applied for DDR5 SDRAM Input Signals during Connectivity Test Mode.

Table 59 — CMOS rail to rail Input Levels for TEN

Parameter	Symbol	Min	Max	Unit	Notes
TEN AC Input High Voltage	VIH(AC)_TEN	0.8 * VDD	VDD	V	1
TEN DC Input High Voltage	VIH(DC)_TEN	0.7 * VDD	VDD	V	
TEN DC Input Low Voltage	VIL(DC)_TEN	VSS	0.3 * VDD	V	
TEN AC Input Low Voltage	VIL(AC)_TEN	VSS	0.2 * VDD	V	2
TEN Input signal Falling time	TF_input_TEN	-	10	ns	
TEN Input signal Rising time	TR_input_TEN	-	10	ns	

NOTE:
1. Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
2. Undershoot might occur. It should be limited by Absolute Maximum DC Ratings.

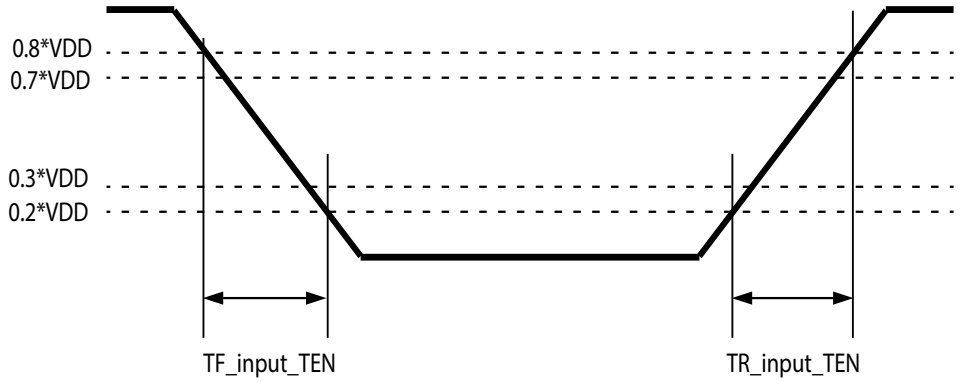


Figure 34 — TEN Input Slew Rate Definition

Table 60 — Single-Ended AC and DC Input levels for CS_n, CA[13:0], CK_t, CK_c, ALERT_n

Parameter	Symbol	Min	Max	Unit	Notes
CTip AC Input High Voltage	VIH(AC)_CTip	VREFCA + 0.25	Note 1	V	
CTip DC Input High Voltage	VIH(DC)_CTip	VREFCA + 0.15	VDD	V	
CTip DC Input Low Voltage	VIL(DC)_CTip	VSS	VREFCA - 0.15	V	
CTip AC Input Low Voltage	VIL(AC)_CTip	Note 1	VREFCA - 0.25	V	
CTip Input signal Falling time	TF_input_CTip	-	5	ns	
CTip Input signal Rising time	TR_input_CTip	-	5	ns	

NOTE:
1 .See TBD Sections “Overshoot and Undershoot Specifications”.

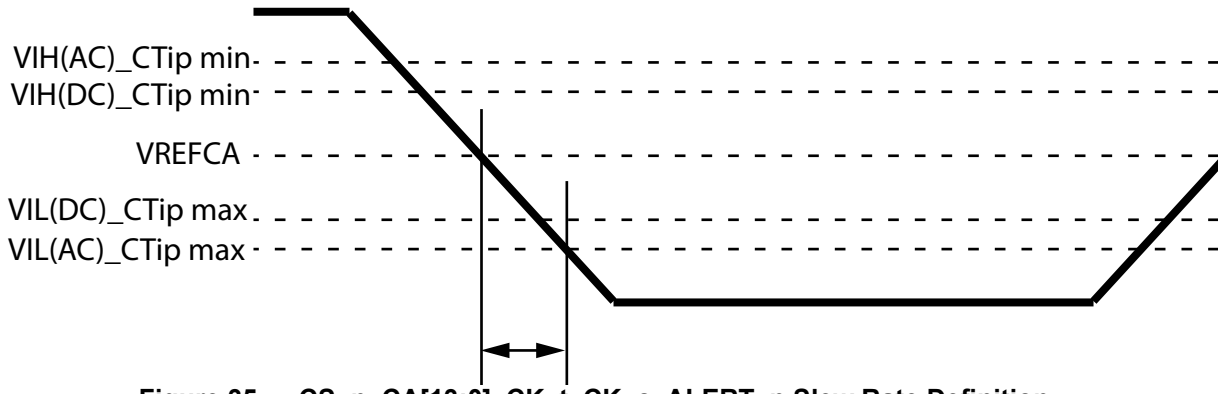


Figure 35 — CS_n, CA[13:0], CK_t, CK_c, ALERT_n Slew Rate Definition

4.18.5.1 Input Levels for RESET_n

RESET_n input condition is the same as normal operation, refer to TBD Section.

4.19 ZQ Calibration Commands - Q1'17 Ballot #1845.18

4.19.1 ZQ Calibration Description

The MPC command is used to initiate ZQ Calibration, which calibrates the output driver impedance across process, temperature, and voltage. ZQ Calibration occurs in the background of device operation.

There are two ZQ Calibration modes initiated with the MPC command: ZQCal Start, and ZQCal Latch. ZQCal Start initiates the SDRAM's calibration procedure, and ZQCal Latch captures the result and loads it into the SDRAM's drivers.

A ZQCal Start command may be issued anytime the DDR5-SDRAM is not in a power-down state. There are two timing parameters associated with ZQ Calibration. tZQCAL is the time from when the ZQCal Start MPC command is sent to when the host can send the ZQCal Latch MPC command. tZQLAT is the time from when the ZQCal Latch MPC command is sent by the host to when the CA bus (and subsequently the DQ bus) can be used for normal operation. A ZQCal Latch Command may be issued anytime outside of power-down after tZQCAL has expired and all DQ bus operations have completed. The CA Bus must maintain a Deselect state during tZQLAT to allow CA ODT calibration settings to be updated.

After a ZQCal Start and until tZQCAL finishes, neither another ZQCal Start nor a ZQCal Latch is allowed.

Table 61 — ZQ Calibration timing Parameters

Parameter	Symbol	Min/Max	Value	Unit
ZQ Calibration Time	tZQCAL	MIN	TBD	ns
ZQ Calibration Latch Time	tZQLAT	MIN	TBD	ns

4.19.2 ZQ External Resistor, Tolerance, and Capacitive Loading

To use the ZQ calibration function, a 240 ohm +/- 1% tolerance external resistor must be connected between the ZQ pin and V_{DDQ}.

If the system configuration has more than one rank, and if the ZQ pins of both ranks are attached to a single resistor, then the SDRAM controller must ensure that the ZQCal's don't overlap.

The total capacitive loading on the ZQ pin must be limited to 25pF.

4.20 VrefCA Command - Q4'16 Ballot Proposal

4.20.1 Introduction

The VrefCA setting must be set prior to training the CS_n and CA bus timings relative to CK. In order to accomplish this, DDR5-SDRAM's will support a single UI command specifically for setting the VrefCA setting. This avoids any timing and/or default VrefCA setting issues with sending a 2UI MRW command, by enabling the host to extend the setup and hold time for the CA signals. In addition, the VrefCA command will support multiple cycles of CS_n assertion. The multiple cycles of CS_n assertion ensures the DRAM will capture the VrefCA command during at least one rising CK_t/CK_c edge.

Table 62 — VrefCA Command Definition

Function	Abbreviation	CS	CA Pins													NOTES
			CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13	
Vref CA Command	VrefCA	L	H	H	L	L	L	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	V	

4.20.2 VrefCA Command Timing

The following diagram illustrates a timing sequence example for the VrefCA command that occurs prior to CS and CA training. The command is sampled on every rising edge of CK_t/CK_c. The host must ensure that the CA signals are valid during the entire CS_n assertion time. The timing of the CS_n assertion may not satisfy the setup/hold requirements around all CK_t/CK_c transitions, but it will satisfy the setup/hold requirements relative to at least one CK_t/CK_c rising edge.

There is no separate mode that enables the multi-cycle CS_n assertion. This timing relationship can always be used by the host to send the VrefCA commands even after training has been completed for the interface.

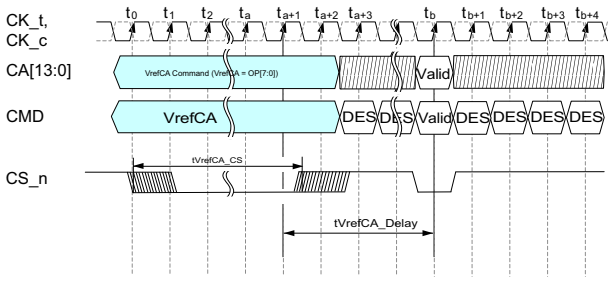


Figure 36 — Timing Diagram for VrefCA Command

Table 63 — AC parameters for VrefCA Comand

Symbol	Description	Min	Max	Unit	Note
tVrefCA_Delay	VrefCA command to any other valid command delay	TBD	-	nCK	
tVrefCA_CS	Time CS_n is held low to register VrefCA command	3.5	TBD	nCK	1,2

NOTE:
1 - Multiple cycles are used to avoid possible metastability of CS_n.
2 - At the end of CSTM, it is assumed that the host should be able to place the CS_n appropriately and the VrefCA command could be issued as a single cycle command.

4.21 CA Vref Training Specification - Q2'17 Ballot #1830.73A w/Editorial Updates

The DRAM internal CA Vref specification parameters are voltage operating range, stepsize, Vref set tolerance, Vref step time and Vref valid level.

The voltage operating range specifies the minimum required Vref setting range for DDR5 DRAM devices. The minimum range is defined by Vrefmax and Vrefmin as depicted in Figure 37 below.

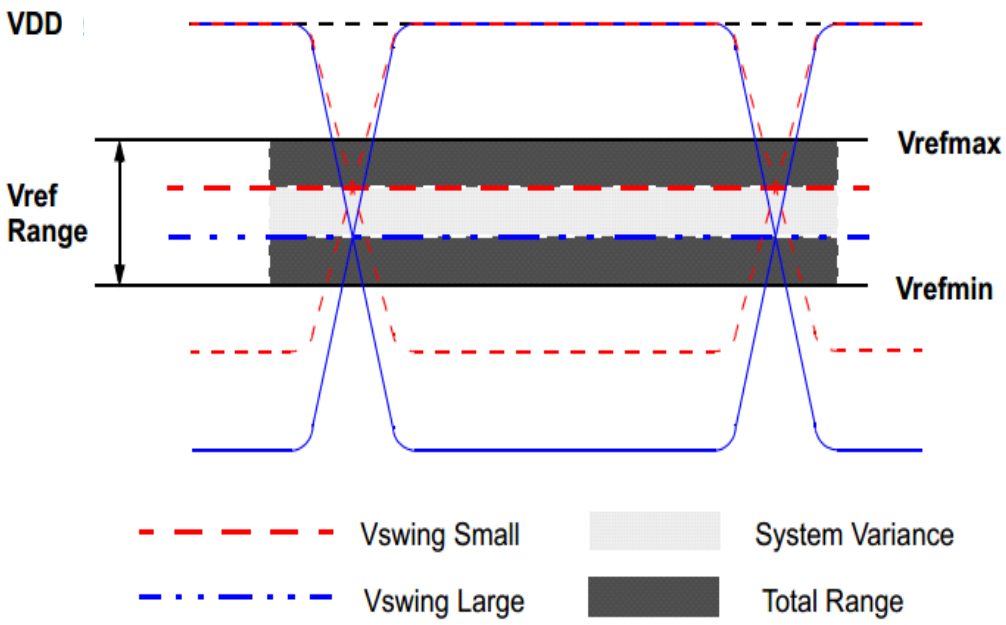


Figure 37 — Vref operating range(Vrefmin, Vrefmax)

The Vref stepsize is defined as the stepsize between adjacent steps. For a given design the DRAM Vref step size must be within the range specified.

The Vref set tolerance is the variation in the Vref voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for Vref set tolerance uncertainty. The range of Vref set tolerance uncertainty is a function of number of steps n.

The Vref set tolerance is measured with respect to the ideal line which is based on the two endpoints. Where the endpoints are at the min and max Vref values for a specified range. An illustration depicting an example of the stepsize and Vref set tolerance is below.

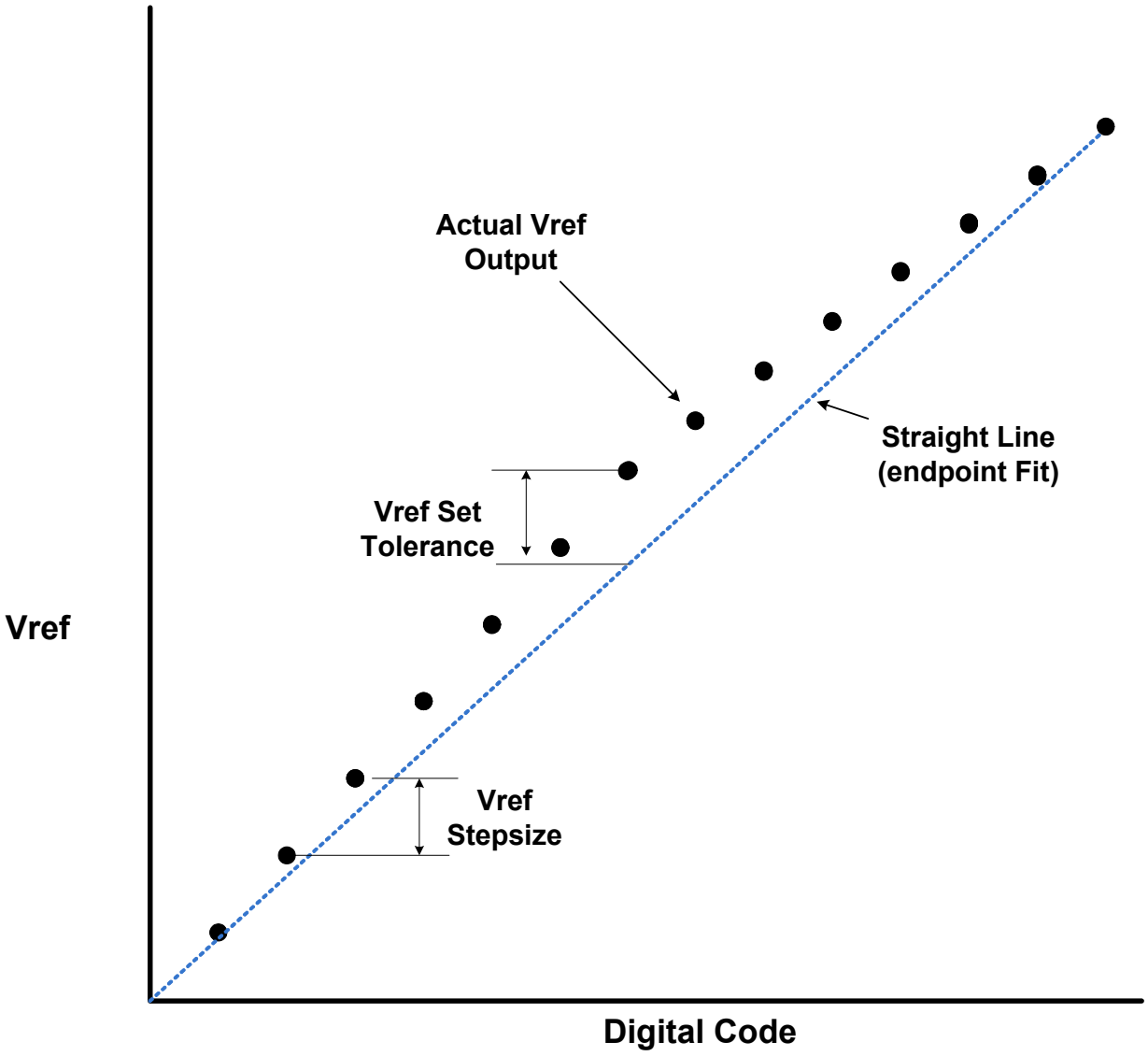


Figure 38 — Example of Vref set tolerance (max case only shown) and stepsize

The Vref increment/decrement step times are defined by Vref_time. The Vref_time is defined from t0 to t1 as shown in the Figure 39 below where t1 is referenced to when the Vref voltage is at the final DC level within the Vref valid tolerance (Vref_val_tol).

The Vref valid level is defined by Vref_val tolerance to qualify the step time t1 as shown in Figure 39. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any Vref increment/decrement adjustment. This parameter is only applicable for DRAM component level validation/characterization.

t0 - is referenced to Vref command clock

t1 - is referenced to the Vref_val_tol

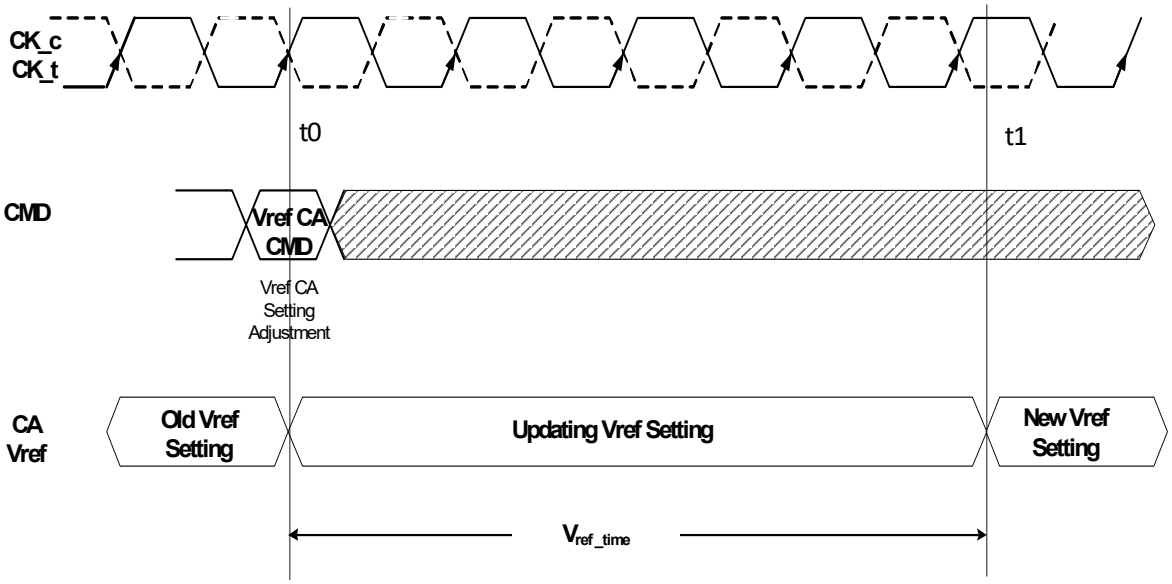


Figure 39 — Vref_time timing diagram

The minimum time required between two Vref commands is Vref_time.

Table 64 — VREF CA Mode Register

MR Address	MRW OP	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR11	UI	RFU CA VREF Setting							

A Vref CA command is used to store the VREF values into the VREF CA MR11. This mode register is only programmed via the command but is readable via a normal MRR.

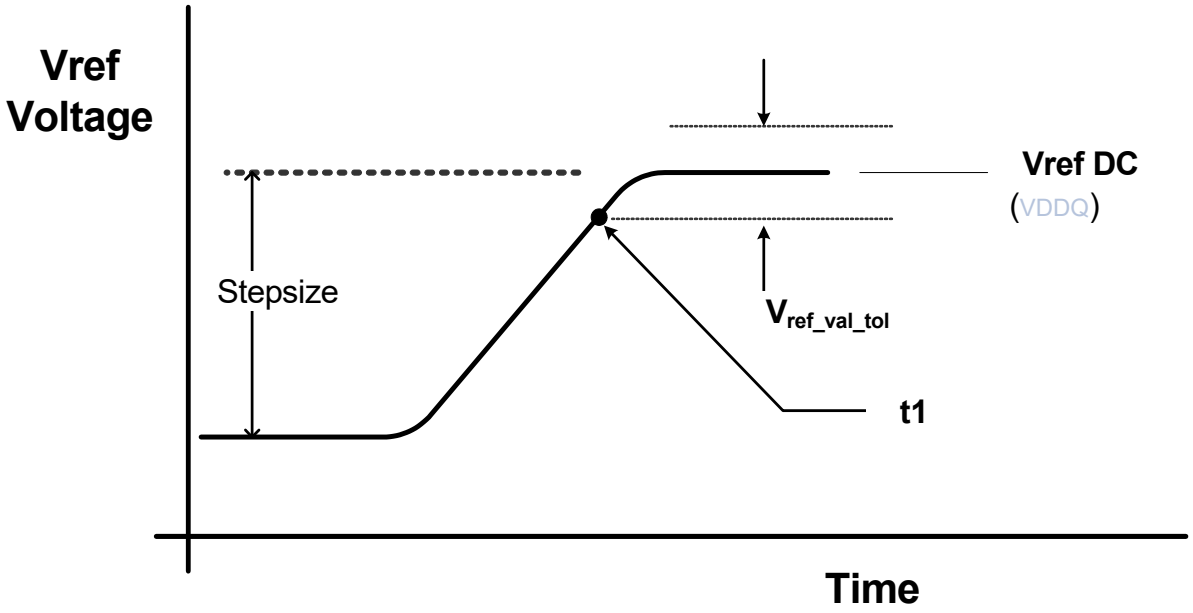


Figure 40 — Vref step single stepsize increment case.

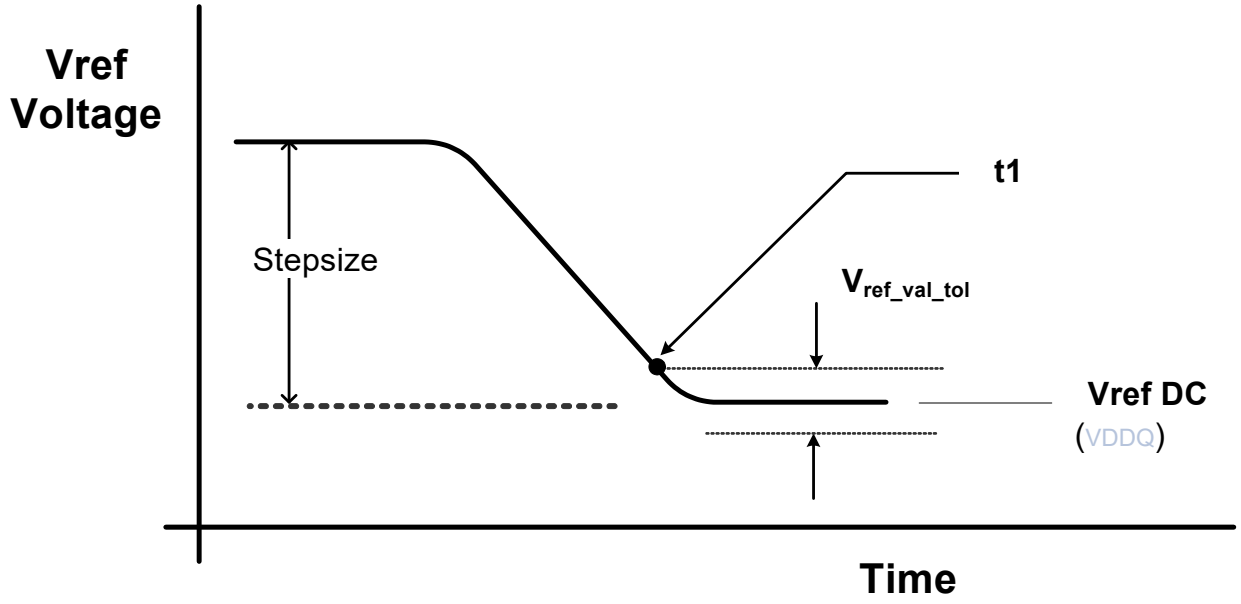


Figure 41 — Vref step single stepsize decrement case

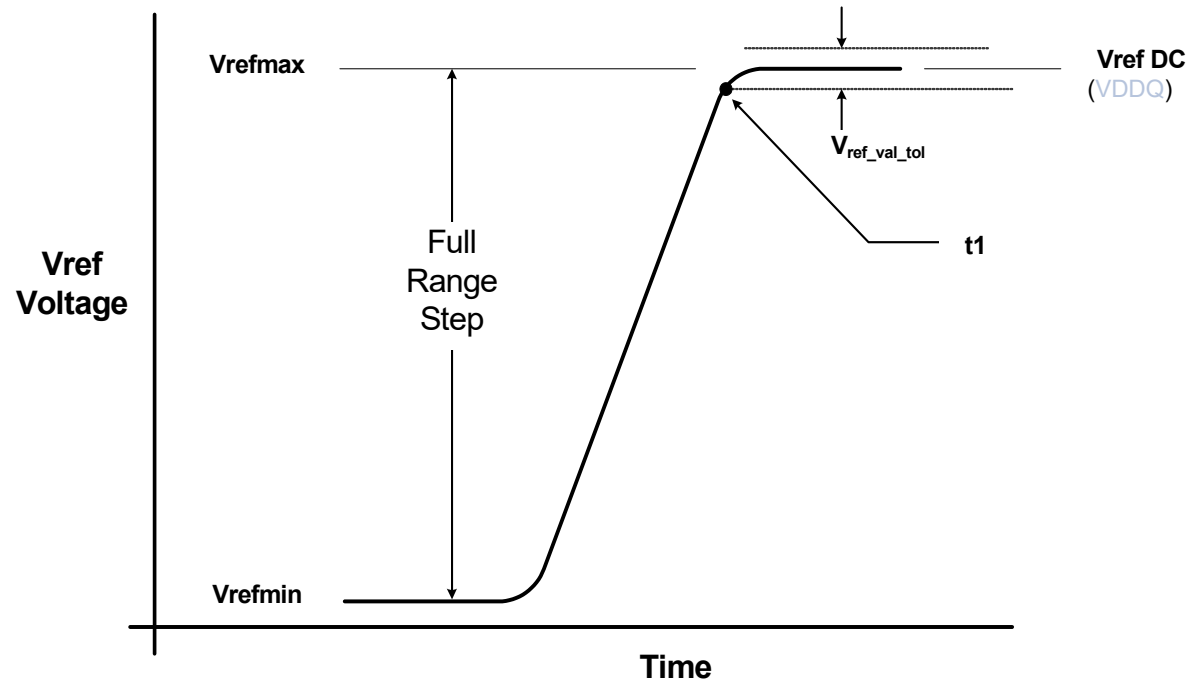


Figure 42 — Vref full step from Vrefmin to Vrefmax case

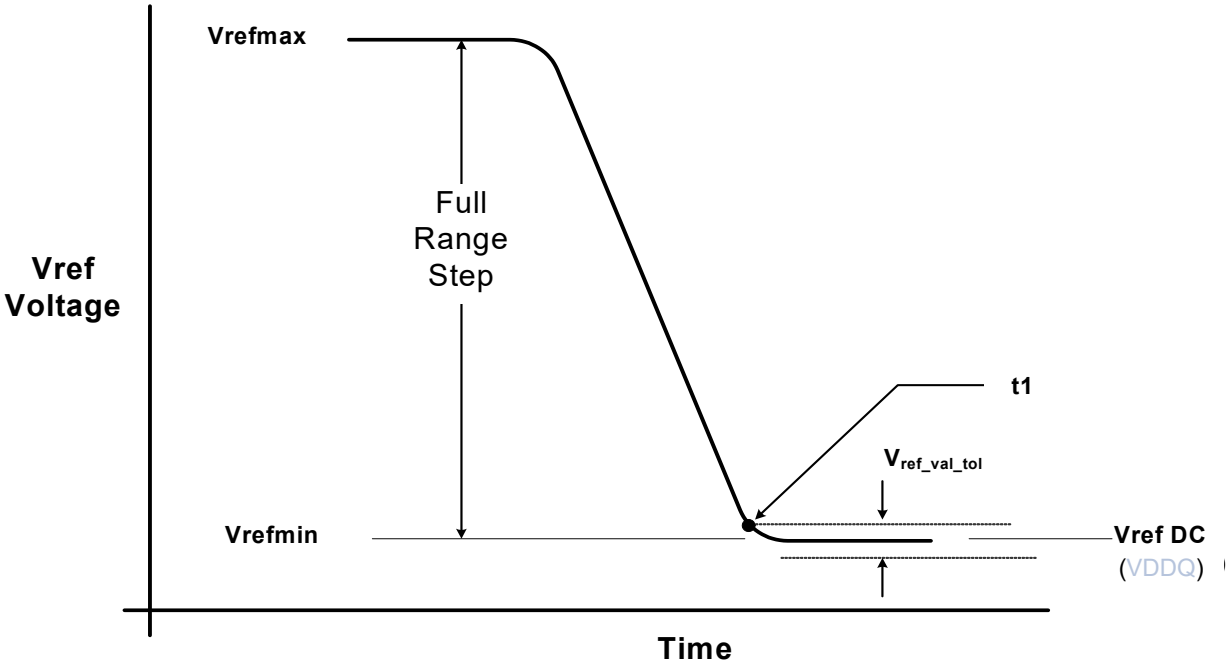


Figure 43 — Vref full step from Vrefmax to Vrefmin case.

The table below contains the CA internal vref specifications that will be characterized at the component level for compliance. The component level characterization method is tbd.

Table 65 — CA Internal VREF Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Vref Max operating point	V_{ref_max}	97.5%	-	-	VDDQ	1
Vref Min operating poin	V_{ref_min}	-	-	45%	VDDQ	1
Vref Stepsize	V_{ref_step}	0.41%	0.50%	0.59%	VDDQ	2
Vref Set Tolerance	$V_{ref\_set\_tol}$	-1.625%	0.00%	1.625%	VDDQ	3,4,6
	$V_{ref\_set\_tol}$	-0.15%	0.00%	0.15%	VDDQ	3,5,7
Vref Step Time	V_{ref_time}	-	-	150	ns	8
Vref Valid Tolerance	$V_{ref\_val\_tol}$	-0.15%	0.00%	0.15%	VDDQ	9

NOTES:

1 - Vref DC voltage referenced to VDDQ_DC.

2 - Vref stepsize increment/decrement range. Vref at DC level.

3 - Vref_new = Vref_old $\pm$ n*Vref_step; n= number of steps; if increment use "+"; If decrement use "-"

4 - The minimum value of Vref setting tolerance = Vref_new - 1.625%*VDDQ. The maximum value of Vref setting tolerance = Vref_new + 1.625%*VDDQ. For n>4

5 - The minimum value of Vref setting tolerance = Vref_new - 0.15%*VDDQ. The maximum value of Vref setting tolerance = Vref_new + 0.15%*VDDQ. For n$\leq$ 4

6 - Measured by recording the min and max values of the Vref output over the range, drawing a straight line between those points and comparing all other Vref output settings to that line

7 - Measured by recording the min and max values of the Vref output across 4 consecutive steps(n=4), drawing a straight line between those points and comparing all other Vref output settings to that line

8 - Time from Vref command to increment or decrement

9 -Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. Vref valid is to qualify the step times which will be characterized at the component level

4.22 DQ Vref Training Specification - Q2'17 Ballot #1849.14 w/Editorial Updates

The DRAM internal DQ Vref specification parameters are voltage operating range, stepsize, Vref set tolerance, Vref step time and Vref valid level.

The voltage operating range specifies the minimum required Vref setting range for DDR5 DRAM devices. The minimum range is defined by Vrefmax and Vrefmin as depicted in Figure 44 below.

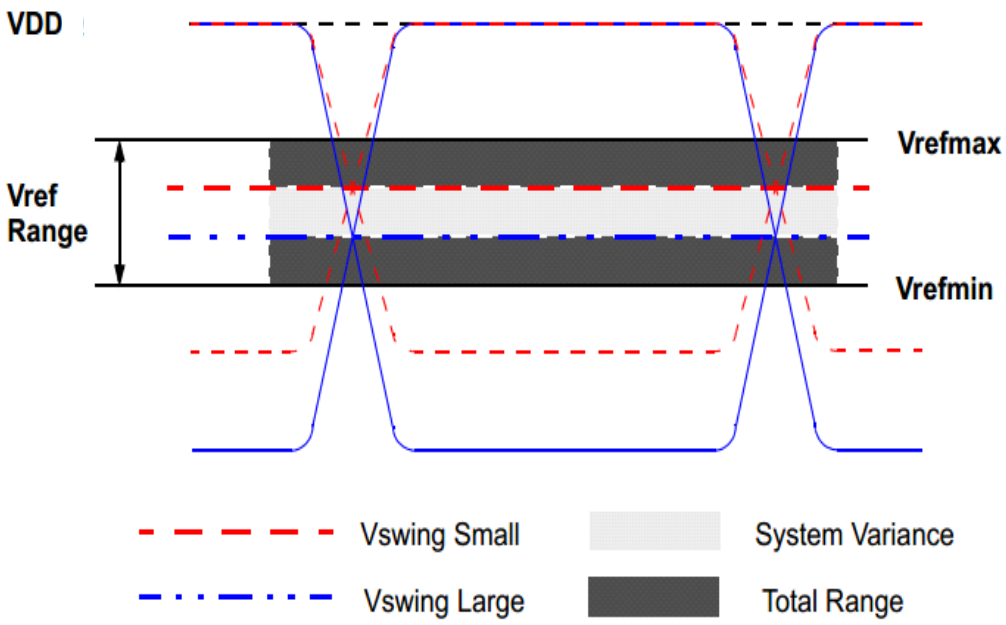


Figure 44 — Vref operating range(Vrefmin, Vrefmax)

The Vref stepsize is defined as the stepsize between adjacent steps. For a given design the DRAM Vref step size must be within the range specified.

The Vref set tolerance is the variation in the Vref voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for Vref set tolerance uncertainty. The range of Vref set tolerance uncertainty is a function of number of steps n.

The Vref set tolerance is measured with respect to the ideal line which is based on the two endpoints. Where the endpoints are at the min and max Vref values for a specified range. An illustration depicting an example of the stepsize and Vref set tolerance is below.

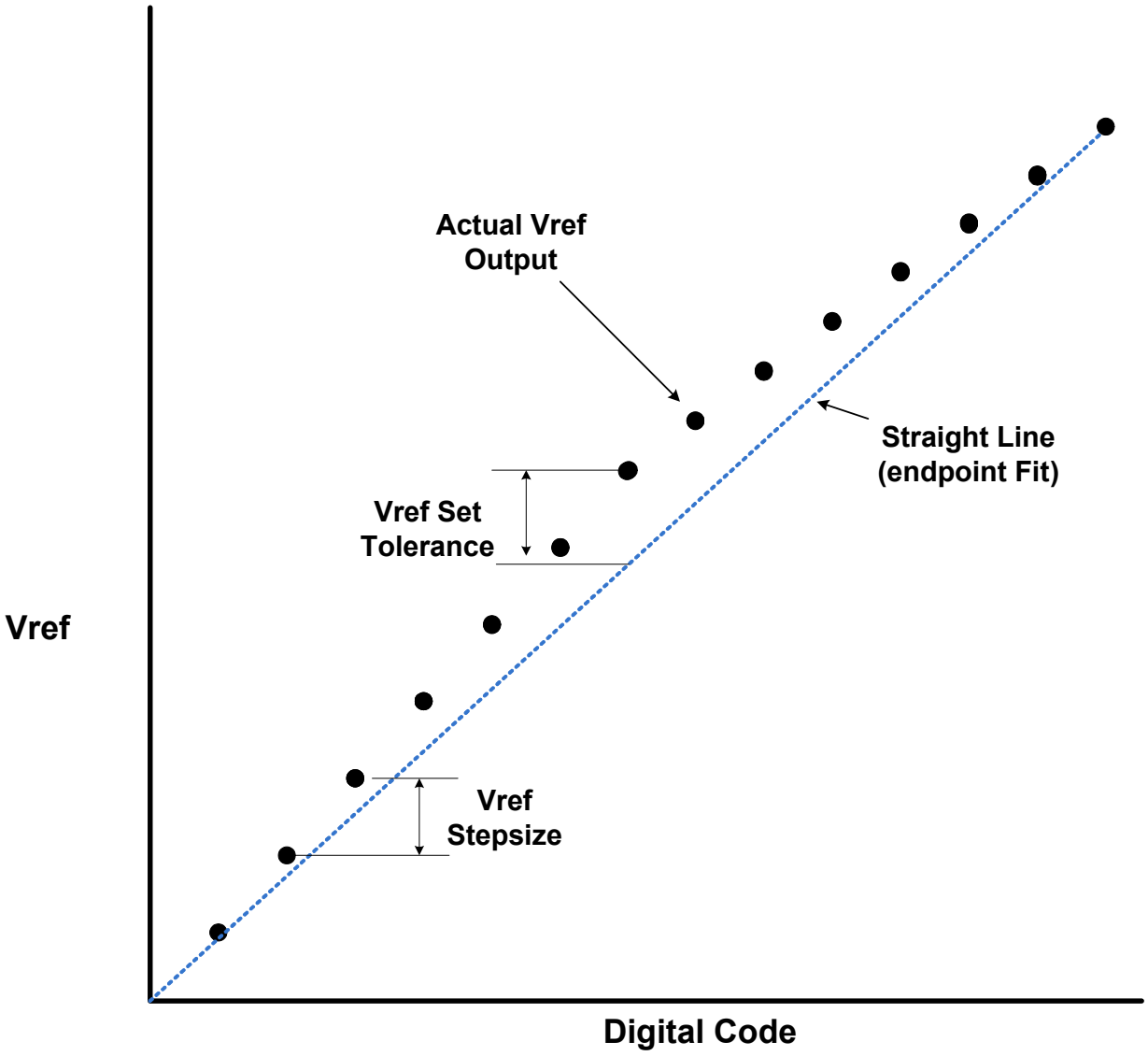


Figure 45 — Example of Vref set tolerance (max case only shown) and stepsize

The Vref increment/decrement step times are defined by Vref_time. The Vref_time is defined from t0 to t1 as shown in the Figure 46 below where t1 is referenced to when the Vref voltage is at the final DC level within the Vref valid tolerance (Vref_val_tol).

The Vref valid level is defined by Vref_val tolerance to qualify the step time t1 as shown in Figure 46. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any Vref increment/decrement adjustment. This parameter is only applicable for DRAM component level validation/characterization.

t0 - is referenced to Vref command clock

t1 - is referenced to the Vref_val_tol

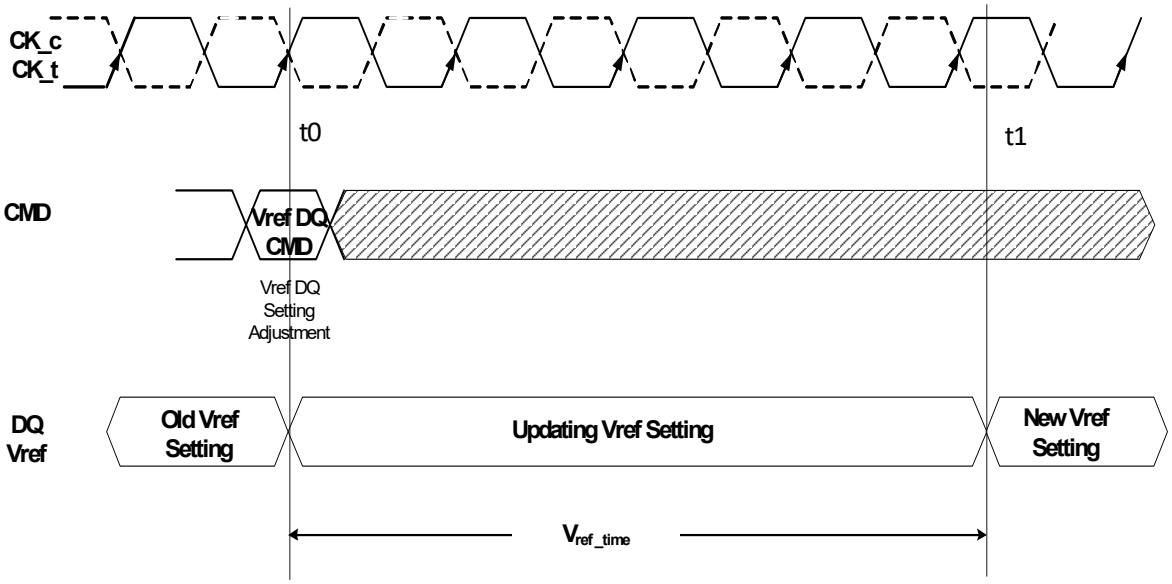


Figure 46 — Vref_time timing diagram

The minimum time required between two Vref commands is Vref_time.

Table 66 — VREF DQ Mode Register

MR Address	MRW OP	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR10	UI	RFU	DQ VREF Setting						

A Vref DQ command is used to store the VREF values into the VREF DQ MR10. This mode register is only programmed via the command but is readable via a normal MRR.

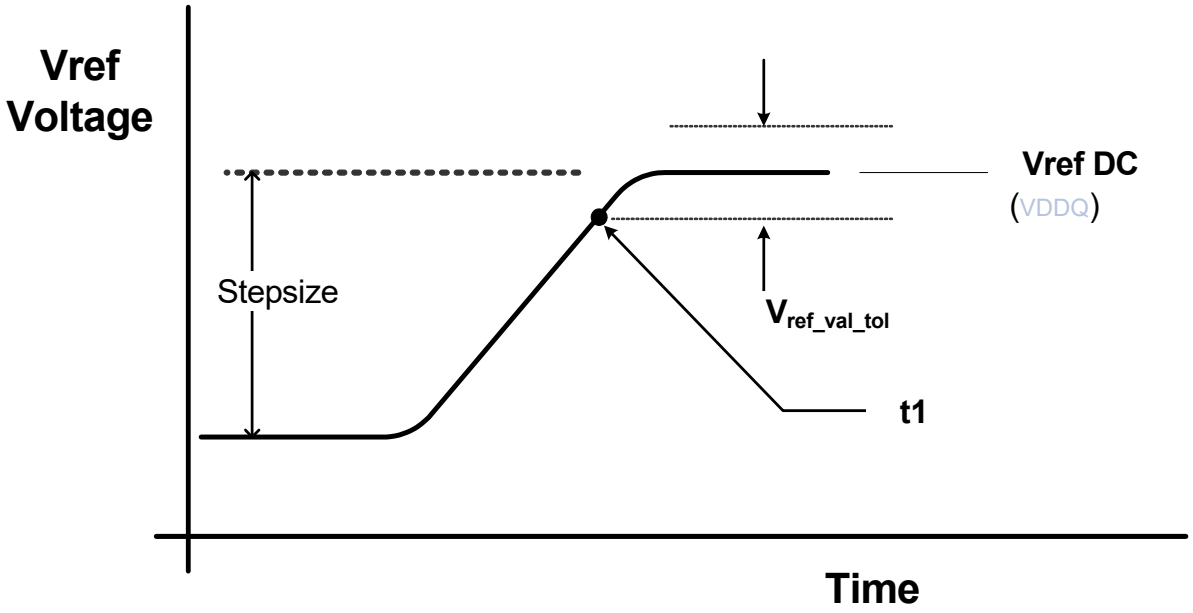


Figure 47 — Vref step single stepsize increment case.

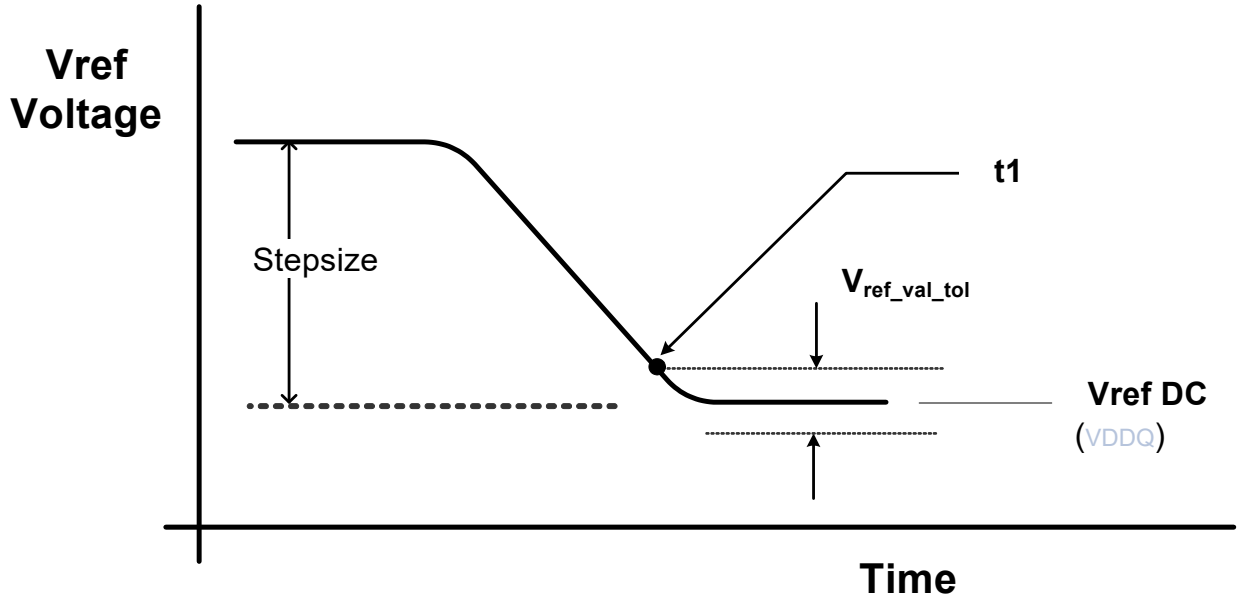


Figure 48 — Vref step single stepsize decrement case

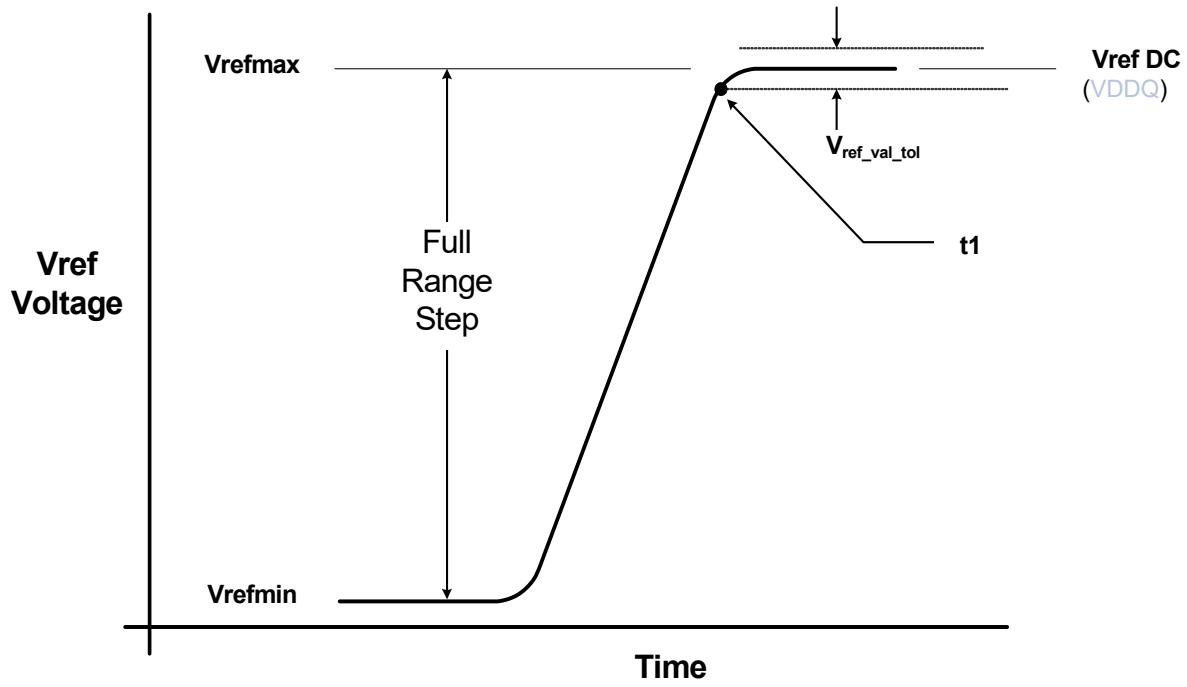


Figure 49 — Vref full step from Vrefmin to Vrefmax case

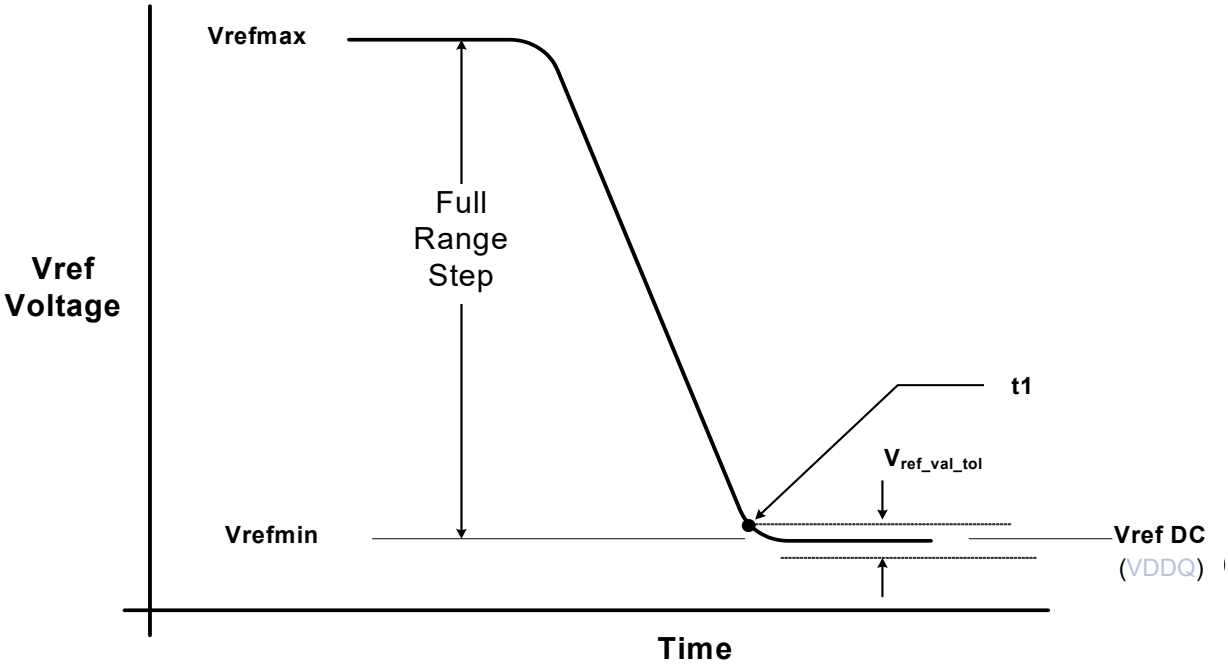


Figure 50 — Vref full step from Vrefmax to Vrefmin case.

The table below contains the DQ internal Vref specifications that will be characterized at the component level for compliance. The component level characterization method is tbd.

Table 67 — DQ Internal VREF Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Vref Max operating point	V_{ref_max}	97.5%	-	-	VDDQ	1
Vref Min operating point	V_{ref_min}	-	-	45%	VDDQ	1
Vref Stepsize	V_{ref_step}	0.41%	0.50%	0.59%	VDDQ	2
Vref Set Tolerance	$V_{ref\_set\_tol}$	-1.625%	0.00%	1.625%	VDDQ	3,4,6
	$V_{ref\_set\_tol}$	-0.15%	0.00%	0.15%	VDDQ	3,5,7
Vref Step Time	V_{ref_time}	-	-	150	ns	8
Vref Valid Tolerance	$V_{ref\_val\_tol}$	-0.15%	0.00%	0.15%	VDDQ	9

NOTES:

1 - Vref DC voltage referenced to VDDQ_DC.

2 - Vref stepsize increment/decrement range. Vref at DC level.

3 - Vref_new = Vref_old $\pm$ n*Vref_step; n= number of steps; if increment use "+"; If decrement use "-"

4 - The minimum value of Vref setting tolerance = Vref_new - 1.625%*VDDQ. The maximum value of Vref setting tolerance = Vref_new + 1.625%*VDDQ. For n>4.

5 - The minimum value of Vref setting tolerance = Vref_new - 0.15%*VDDQ. The maximum value of Vref setting tolerance = Vref_new + 0.15%*VDDQ. For n$\leq$ 4.

6 - Measured by recording the min and max values of the Vref output over the range, drawing a straight line between those points and comparing all other Vref output settings to that line.

7 - Measured by recording the min and max values of the Vref output across 4 consecutive steps(n=4), drawing a straight line between those points and comparing all other Vref output settings to that line.

8 - Time from Vref command to increment or decrement.

9 - Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. Vref valid is to qualify the step times which will be characterized at the component level.

4.23 Post Package Repair (PPR) - Q3'17 Ballot #1830.51

DDR5 supports Fail Row address repair, PPR which allows a simple and easy repair method in a system. Two methods are provided: Hard Post Package Repair (hPPR) for a permanent Row repair and Soft Post Package Repair (sPPR) for a temporary Row repair.

Entry into hPPR or sPPR is protected through a sequential MRS guard key to prevent unintentional hPPR programming. The sequential MRS guard key is the same for both hPPR and sPPR.

The hPPR/sPPR guard key requires a sequence of four MRW commands to be issued immediately after entering hPPR/sPPR, as shown in Figure 51. The guard key sequence must be entered in the specified order as stated and shown in the spec below and in Table 69. Any interruptions of the guard key sequence from other MRW/R commands or non-MR commands such as ACT, WR, RD is not allowed. Although interruption of the guard key entry is not allowed, if the guard key is not entered in the required order or is interrupted by other commands, the hPPR mode or sPPR mode will not execute and the offending command terminated the hPPR/sPPR entry may or may not execute correctly however the offending command will not cause the DRAM to lock up. Additionally when the hPPR entry sequence is interrupted subsequent ACT and WR commands will be conducted as normal DRAM commands. If a hPPR operation was prematurely terminated, the MR26 OP[5] and OP[7] must be reset to "0" prior to perform another hPPR or sPPR operation. The DRAM does not provide an error indication if an incorrect hPPR/sPPR guard key sequence is entered.

Figure 51 — Guard Key Timing Diagram

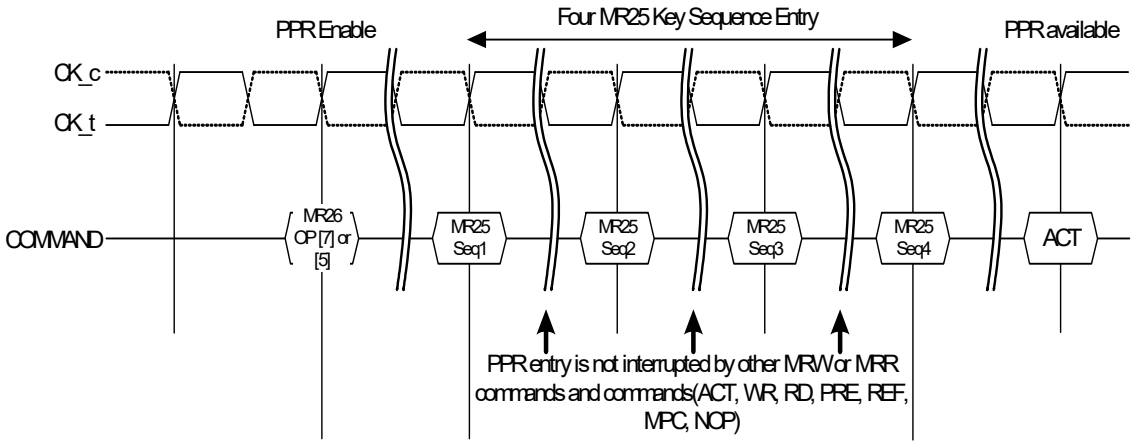


Table 68 — Guard Key Encoding for MR 25

Guard Keys	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]	Notes
MR25 Seq1	**1**	**1**	**0**	**0**	**1**	**1**	**1**	**1**	
MR25 Seq2	**0**	**1**	**1**	**1**	**0**	**0**	**1**	**1**	
MR25 Seq3	**1**	**0**	**1**	**1**	**1**	**0**	**1**	**1**	
MR25 Seq4	**0**	**0**	**1**	**1**	**1**	**0**	**1**	**1**	

4.23.1 Hard PPR (hPPR) - Q3'16 Ballot #1830.51

With hPPR, DDR5 can correct one Row address per Bank Group and the Electrical-fuse cannot be switched back to un-fused states once it is programmed. The controller should prevent unintended the hPPR mode entry and repair. (i.e. During the Command/ Address training period). Entry into hPPR is through a register enable, ACT command is used to transmit the bank and row address of the row to be replaced in DRAM. After tRCD time, a WR command is used to select the individual DRAM through the DQ bits and to transfer the repair address to the DRAM. After program time, and PRE, the hPPR mode can be exited and normal operation can resume.

4.23.1.1 hPPR Fail Row Address Repair

The following is procedure of hPPR.

1.Before entering 'hPPR' mode, All banks must be Precharged

2.Enable hPPR using MR26 bit "OP[7]=1" and wait tMOD

3. Issue guard key as four consecutive MR25 OP[7:0] MRW commands each with a unique address field OP[7:0]. Each MRW command should be spaced by tMOD.

4. Issue ACT command with the Bank and Row fail address. Write data is used to select the individual DRAM in the rank for repair. Issue ACT command with Fail Row address

5. After tRCD, Issue WR with VALID address. DRAM will consider Valid address with WR command as 'Don't Care'

6. After WL(WL=CWL+AL+PL), All DQs of Target DRAM should be LOW for 4tCK. If HIGH is driven to All DQs of a DRAMs for 4tCK, then DRAM does not conduct hPPR and retains data if REF command is properly issued; if all DQs are neither all LOW nor all HIGH for 4tCK, then hPPR mode execution is unknown.

7. Wait tPGM to allow DRAM repair target Row Address internally and issue PRE

8. Wait tPGM_Exit after PRE which allow DRAM to recognize repaired Row address

9. Exit hPPR with setting MR26 bit "OP7=0"

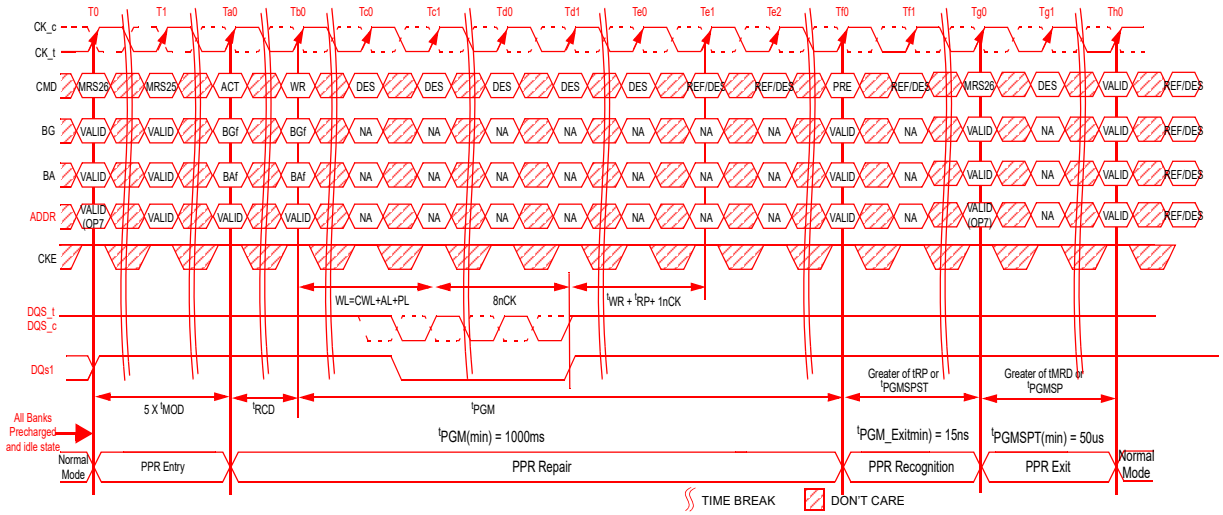
10. DDR5 will accept any valid command after tPGMPST

11. In the case of multiple addresses to be repaired, Repeat Step 2 to 9

During hPPR mode, REF, REFsb commands are allowed, but array contents are not guaranteed. Upon receiving a REF or REFsb command in hPPR mode, the DRAM may ignore the Refresh operation but will not disrupt the repair operation. Other commands except REF/REFsb during tPGM can cause incomplete repair so no other command except REF is allowed during tPGM.

Once hPPR mode is exited, to confirm if target row is repaired correctly, host can verify by writing data into the target row and reading it back after hPPR exit with MR26 OP[7] and tPGMPST

Figure 52 — hPPR Fail Row Repair



Note1. Allow REF(1X) from PL+WL+BL/2+tWR+tRP after WR, but does not guarantee array contents are refreshed during hPPR
Note2. Timing diagram shows possible commands but not all shown can be issued at same time; for example if REF is issued at Te1, DES must be issued at Te2 as REF would be illegal at Te2. Likewise, DES must be issued tRFC prior to PRE at Tf0. All regular timings must still be satisfied.

Table 69 — MR Register Bits for PPR

Mode Register	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]	Notes
MR25	PPR Guard Key								
MR26	hPPR Enable	RFU	sPPR Enable	RFU	RFU	RFU	RFU	RFU	

4.23.1.2 Required Timing Parameters

Repair requires additional time period to repair Fail Row Address into spare Row address and the followings are requirement timing parameters for PPR.

Table 70 — PPR Timings

		DDR5-3200/x/y		Unit	Note
Parameter	Symbol	min	max		
hPPR Programming Time: x4/x8	tPGMa	1,000	-	ms	
hPPR Programming Time: x16	tPGMb	2,000	-	ms	
hPPR or sPPR Exit Time	tPGM_Exit	15	-	ns	
New Address Setting time	tPGMPST	50	-	us	

4.23.2 Soft Post Package Repair (sPPR) - Q3'16 Ballot #1830.87

Soft Post Package Repair (sPPR) is a way to quickly, but temporarily, repair TBD row element(s) in a Bank Group on a DDR5 DRAM device, contrasted to hPPR which takes longer but is permanent repair of a row element. There are some limitations and differences between Soft Repair and a Hard Repair. Entry into sPPR is through a register enable, ACT command is used to transmit the bank and row address of the row to be replaced in DRAM. After tRCD time, a WR command is used to select the individual DRAM through the DQ bits and to transfer the repair address into an internal register in the DRAM. After a write recovery time and PRE, the sPPR mode can be exited and normal operation can resume. Care must be taken that refresh is not violated for the other rows in the array during soft repair time. Also note that the DRAM will retain the soft repair information inside the DRAM as long as VDD remains within the operating region. If DRAM power is removed or the DRAM is RESET, the soft repair will revert to the un-repaired state. hPPR and sPPR may not be enabled at the same time. sPPR must have been disabled and cleared prior to entering hPPR mode.

With sPPR, DDR5 can repair TBD Row address per Bank Group. When the hPPR resources for a bank group are used up, the bank group has no more available resources for soft PPR. If a repair sequence is issued to a bank group with no repair resource available, the DRAM will ignore the programming sequence.

Table 71 — sPPR vs hPPR

	Soft Repair	Hard Repair	Note
Persistence of Repair	Volatile – Repaired as long as VDD is within Operating Range	Non-Volatile – repair is permanent after the repair cycle.	Soft Repair erased when Vdd removed or device reset.
Length of time to complete repair cycle	WL+4tCK+tWR	tPGMa or tPGMb	A subsequent sPPR can be performed without affecting the hPPR previously performed provided a row is available in that bank group
# of Repair elements	tbd per BG	tbd per BG	Once hPPR is used within a BG, sPPR is no longer supported
Simultaneous use of soft and hard repair within a BG	Previous hard repairs are allowed before soft repair	Any outstanding soft repairs must be cleared before a hard repair	Clearing sPPR occurs by either: (a) powerdown and power-up sequence or (b) Reset and re-initialize.
Repair Sequence	1 method	1 method	
Bank not having row repair retains array data	Yes	No	
Bank having row repair retain array data	Yes	No	

4.23.2.1 sPPR Repair of a Fail Row Address

The following is the procedure of sPPR with WR command. Note that during the soft repair sequence, no refresh is allowed.

1.Before entering 'sPPR' mode, all banks must be Precharged; DBI and CRC Modes must be disabled

2.Enable sPPR using MR26 bit "OP5=1" and wait tMOD

3.Issue Guard Key as four consecutive MRWx commands each with a unique address field OP[7:0] Each MRWx command should space by tMOD. MRWx Guard Key sequence is the same as hPPR in Table xxx

4.Issue ACT command with the Bank and Row Fail address, Write data is used to select the individual DRAM in the Rank for repair.

5.A WR command is issued after tRCD, with VALID column address. The DRAM will ignore the column address given with the WR command.

6.After WL (WL=CWL+AL+PL), all of the DQs of the individual Target DRAM should be LOW for 4tCK. If any DQ is high during 4tCK burst, then the sPPR protocol will not be executed. If more than one DRAM shares the same command bus, DRAMs that are not being repaired should have all of their DQ's driven HIGH for 4tCK. If all of the DQ's are neither all LOW nor all HIGH for 4tCK, then sPPR mode will not be executed.

7.Wait tWR for the internal repair register to be written and then issue PRE to the Bank.

8.Wait 20ns after PRE which allow DRAM to recognize repaired Row address

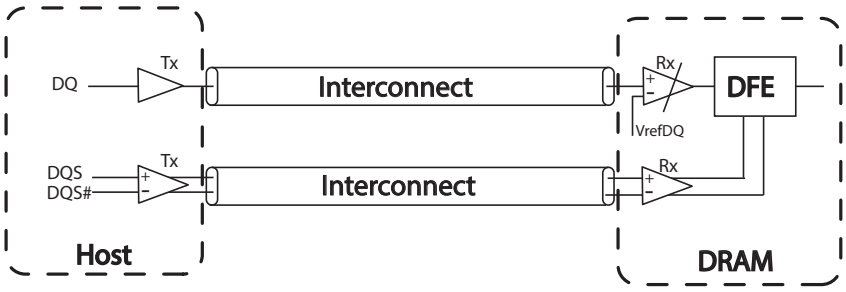
9.Exit PPR with setting MR26 bit "OP5=0" and wait tMOD

4.24 Decision Feedback Equalization - Q4'16 Ballot Proposal

4.24.1 Introduction

At data rates >= 3200MT/s, signal degradation due to Inter Symbol Interference (ISI) is expected to increase and the data eye at the DRAM ball is expected to be closed. Since the memory channel is very reflective due to the many impedance mismatched points that exist along the memory subsystem, ISI due to reflections are expected to increase. Traditional methods of characterizing the Receiver using the input eye mask is no longer sufficient. DDR5 requires equalization to help improve (or open up) the data eyes after the data is latched by the receiver. A 4-tap DFE is chosen to help equalize the DQ signals without amplifying the noise due to insertion loss and reflections, which is a common side effect of other equalization techniques (example CTLE). Figure 53 shows an example of a memory subsystem with DFE circuit included on the DRAM.

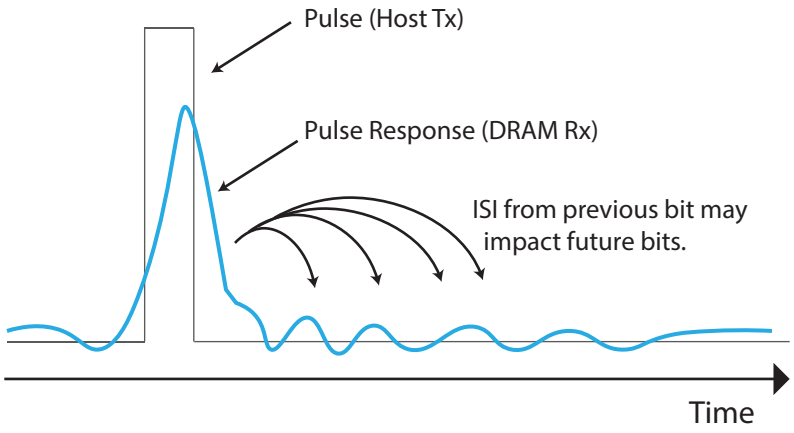
Figure 53 — Example of Memory Subsystem with DFE Circuit on the DRAM



4.24.2 Pulse Response of a Reflective Memory Channel

A reflection dominated channel such as those found in a memory subsystem is anticipated to have substantially reduced data eye at the DRAM ball due to the effects of insertion loss and reflections. Figure represents how a pulse response of a very reflective channel might look like. The attenuation as well as the ringing of the signal can cause the data eye to close at the DRAM ball. Moreover, the ringing can impact future bits that are being sent into the channel, i.e., if the pulse response is for bit n, then the ringing from bit n can impact the signal integrity of future bits n+1, n+2, n+3, n+4, etc. Putting it another way, the signal integrity of any bit, for example bit n, can be impacted by the signals of the previous bits n-1, n-2, n-3, n-4, etc.

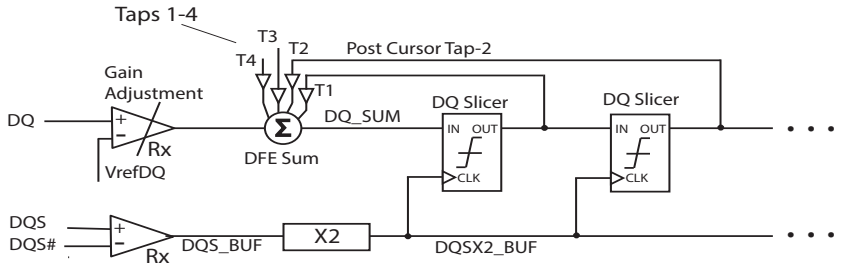
Figure 54 — Example of Pulse Response of a Reflective Channel



4.24.3 Components of the DFE

The 4-tap DFE subsystem consists of a gain amplifier, a DFE summer, 4 DQ slicers (also called Taps) with outputs that loop back to the DFE summer, and a coefficient multiplier for each Tap (Figure 55). The gain control of the front end is used to ensure that the cursor or the current bit is in a congruent relationship with the ISI correction required for the channel. The taps T1, T2, T3, T4 coefficients provide the corrections needed to the current bit by adding or subtracting the effects of ISI of the previous bits.

Figure 55 — 4-Tap DFE Example



The Mode Registers shown in Table 72, ?$paratext>,? on page 233 and Table 73, ?$paratext>,? on page 233 are used by the memory controller to set the strengths of the gain amplifier and the strengths of the correction of the Taps to adapt the ISI cancellation in accordance with the channel performance. Optimal values used for the strengths of the gain amplifier and of the Taps are system dependent, and are usually obtained through a combination of simulations, platform characterizations, and other methods.

Table 72 — Min/Max Ranges for the DFE Gain Adjustment

Description	DDR5 3200-4400			DDR5 4800-6400			Unit	Notes
	Min	Typ	Max	Min	Typ	Max		
DFE Gain Bias Max	6	-	-	6	-	-	dB	1,2,3
DFE Gain Bias Min	-	-	6	-	-	6	dB	1,2,3
DFE Gain Bias Step Size	TBD	2	TBD	TBD	2	TBD	dB	1,2,3
DFE Gain Bias Tolerance	TBD	TBD	TBD	TBD	TBD	TBD	dB	1,2,3
DFE Gain Bias Step Size Tolerance	TBD	TBD	TBD	TBD	TBD	TBD	dB	1,2,3
DFE Gain Bias Tolerance Time	TBD	TBD	TBD	TBD	TBD	TBD	dB	1,2,3

NOTE 1: All parameters are defined over the entire Rx Vref range
NOTE 2: DFE Gain Bias are for all voltage and temperature range
NOTE 3: These values should remain constant voltage and temperature range

Table 73 — Min/Max Ranges for the DFE Tap Coefficients

Description	DDR5 3200-4400			DDR5 4800-6400			Unit	Notes
	Min	Typ	Max	Min	Typ	Max		
DFE Tap-1 Bias Max	50	-	-	50	-	-	mV	1,2,3,4
DFE Tap-1 Bias Min	-	-	-200	-	-	-200	mV	1,2,3
DFE Tap-2 Bias Max	75	-	-	75	-	-	mV	1,2,3
DFE Tap-2 Bias Min	-	-	-75	-	-	-75	mV	1,2,3
DFE Tap-3 Bias Max	60	-	-	60	-	-	mV	1,2,3
DFE Tap-3 Bias Min	-	-	-60	-	-	-60	mV	1,2,3
DFE Tap-4 Bias Max	45	-	-	45	-	-	mV	1,2,3
DFE Tap-4 Bias Min	-	-	-45	-	-	-45	mV	1,2,3
DFE Tap Bias Step Size	TBD	5	TBD	TBD	5	TBD	mV	1,2,3,5
DFE Tap Bias Tolerance	TBD	TBD	TBD	TBD	TBD	TBD	mV	1,2,3,5
DFE Tap Bias Step Size Tolerance	TBD	TBD	TBD	TBD	TBD	TBD	mV	1,2,3,5
DFE Tap Bias Step Time	TBD	TBD	TBD	TBD	TBD	TBD	mV	1,2,3,5

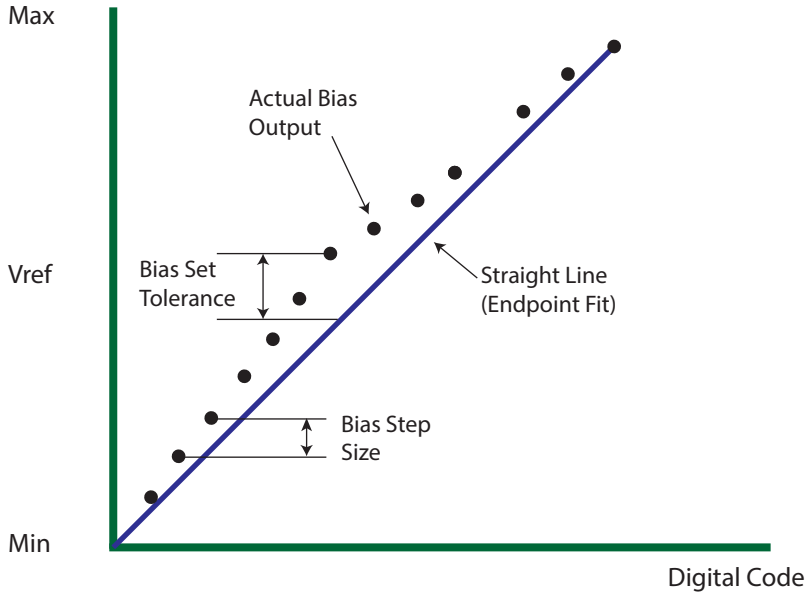
NOTE 1: All parameters are defined over the entire Rx Vref range
NOTE 2: DFE Gain Bias are for all voltage and temperature range
NOTE 3: These values should remain constant voltage and temperature range
NOTE 4: As speed increases, the impact of loss from the channel makes the bias range of the first cursor asymmetric
NOTE 5: It is assumed that the Tap Bias tolerance and Tap Bias Step Size tolerance are identical for Taps 1-4

The DFE Gain Bias step size is defined as the step size between adjacent steps. The DFE Gain Bias step size is TBD with tolerance TBD. However, for a given design, DRAM has one value for the DFE Gain Bias step size that falls within the range. The DFE Gain Bias set tolerance is the variation in the DFE Gain Bias voltage from the ideal setting. This accounts for accumulated error over multiple steps. The range of DFE Gain Bias set tolerance uncertainty is a function of number of steps n.

The DFE Tap Bias step size is TBD with tolerance TBD. However, for a given design, DRAM has one value for the DFE Tap Bias step size that falls within the range. The DFE Tap Bias set tolerance is the variation in the DFE Tap Bias voltage from the ideal setting. This accounts for accumulated error over multiple steps. The range of DFE Tap Bias set tolerance uncertainty is a function of number of steps m.

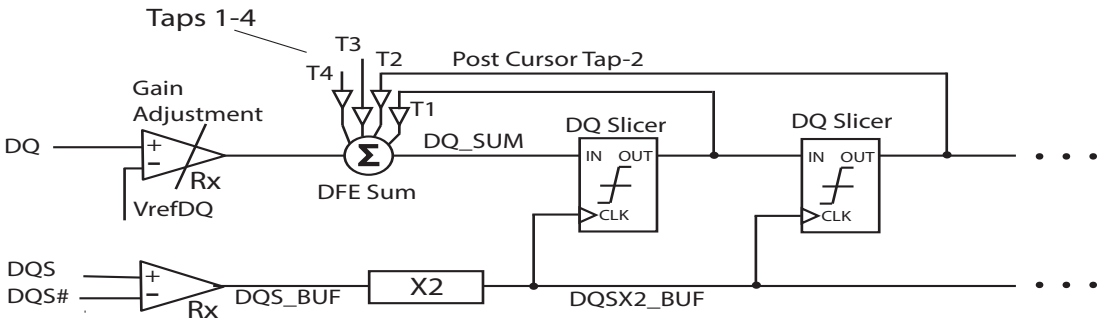
The DFE Gain Bias tolerance and the DFE Tap Bias tolerance are measured with respect to the ideal line, which is based on the two endpoints, where the end points are at the min and max Bias values for a specified range. An illustration depicting an example of the bias set tolerance and step size tolerance is shown in Figure 56 below.

Figure 56 — Example of Bias Tolerances and Step Size



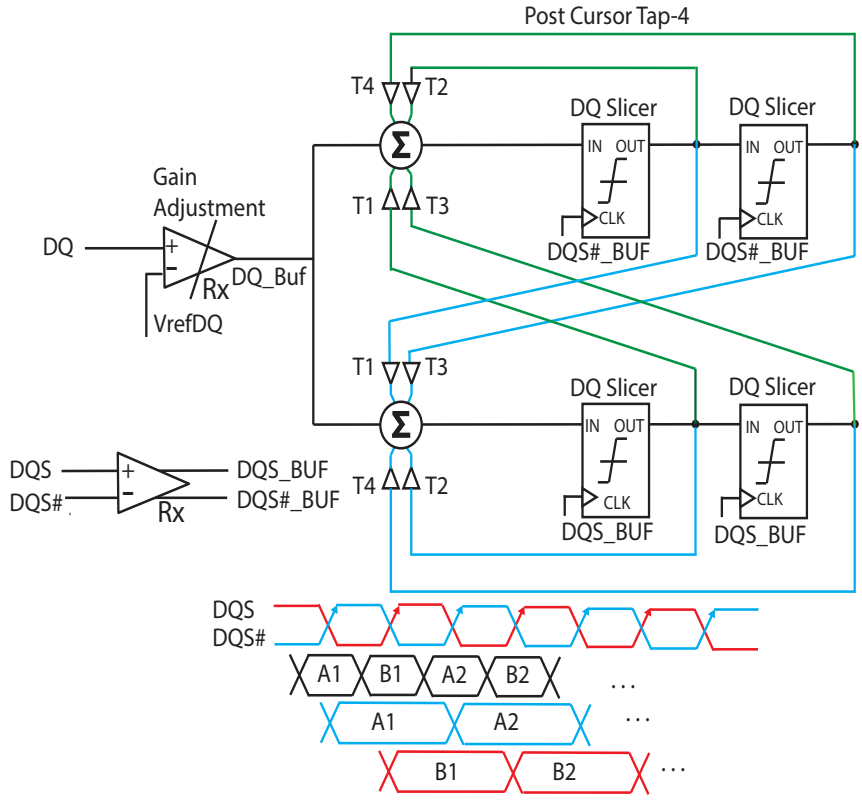
The DRAM may implement 1-way interleave, 2-way interleave, or 4-way interleave 4-tap DFE memory circuitry. The 1-way interleaved 4-tap DFE architecture (Figure 57) requires a strobe multiplier, which is at Nyquist rate, and the output of the DQ slicer runs at same speed as received data.

Figure 57 — 1-Way Interleave 4-Tap DFE Example



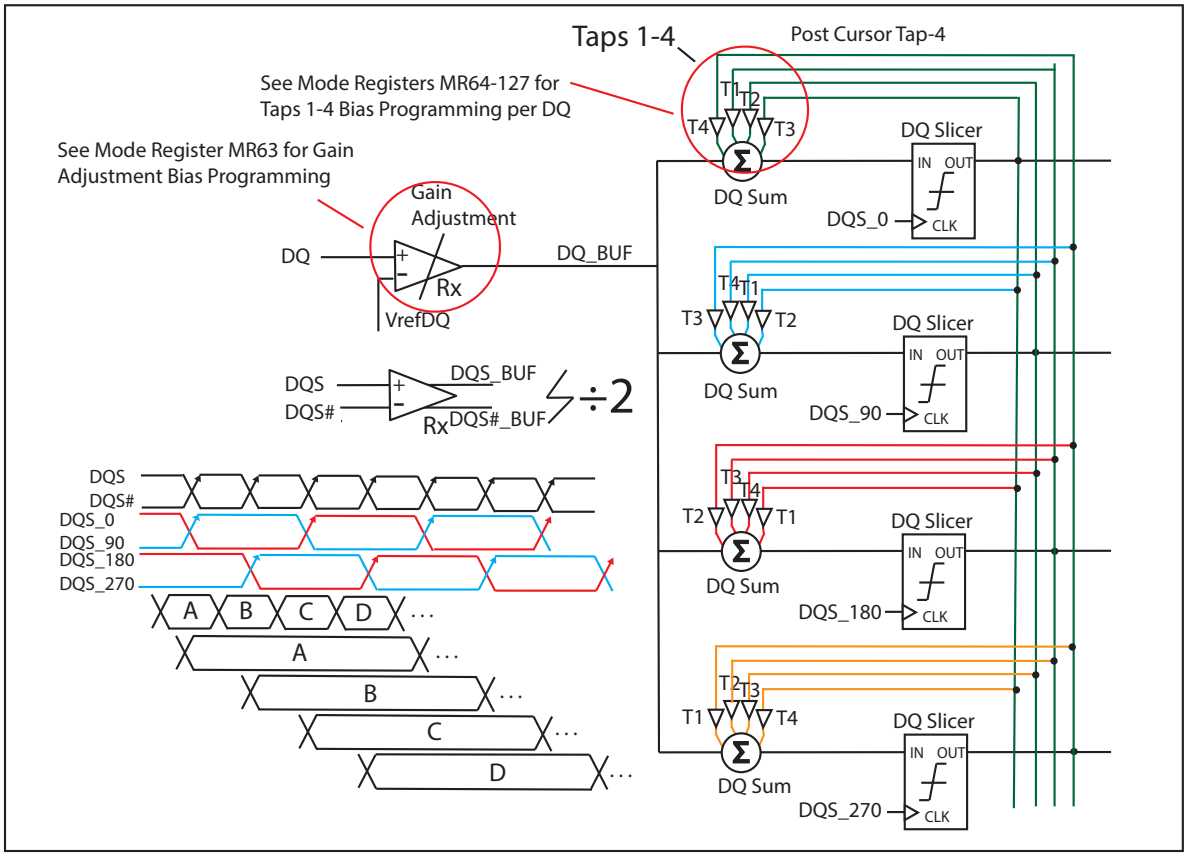
A 2-way interleaved 4-tap DFE architecture (Figure 58) can use the strobe as is. In this case, the output of the DQ slicer runs at half the speed as received data.

Figure 58 — 2-Way Interleave 4-Tap DFE Example



A 4-way interleaved 4-tap DFE architecture (Figure 59) requires a divided clock. In this case, the output of the DQ slicer runs at 1/4 the speed as received data.

Figure 59 — 4-Way Interleave 4-Tap DFE Example



4.25 DQS Interval Oscillator - Q4'16 Ballot #1845.03

As voltage and temperature change on the SDRAM die, the DQS clock tree delay will shift and may require re-training. The DDR5-SDRAM includes an internal DQS clock-tree oscillator to measure the amount of delay over a given time interval (determined by the controller), allowing the controller to compare the trained delay value to the delay value seen at a later time. The DQS Oscillator will provide the controller with important information regarding the need to re-train, and the magnitude of potential error.

The DQS Interval Oscillator is started by issuing a MPC [Start DQS Osc] command with OP[X:X] set as described in the MPC Operation section, which will start an internal ring oscillator that counts the number of time a signal propagates through a copy of the DQS clock tree.

The DQS Oscillator may be stopped by issuing a MPC [Stop DQS Osc] command with OP[X:X] set as described in the MPC Operation section, or the controller may instruct the SDRAM to count for a specific number of clocks and then stop automatically (See MRXX for more information). If MRXX is set to automatically stop the DQS Oscillator, then the MPC [Stop DQS Osc] command should not be used (illegal). When the DQS Oscillator is stopped by either method, the result of the oscillator counter is automatically stored in MRXX and MRXX.

The controller may adjust the accuracy of the result by running the DQS Interval Oscillator for shorter (less accurate) or longer (more accurate) duration. The accuracy of the result for a given temperature and voltage is determined by the following equation:

$$\textit{DQS Oscillator Granularity Error} = \frac{\textit{2 * (DQS delay)}}{\textit{Run Time}}$$

Where:
Run Time = total time between start and stop commands
DQS delay = the value of the DQS clock tree delay (tDQS2DQ min/max)

Additional matching error must be included, which is the difference between DQS training circuit and the actual DQS clock tree across voltage and temperature. The matching error is vendor specific.

Therefore, the total accuracy of the DQS Oscillator counter is given by:

DQS Oscillator Accuracy = 1 - Granularity Error - Matching Error

Example: If the total time between start and stop commands is 100ns, and the maximum DQS clock tree delay is 400ps (tDQS2DQ max), then the DQS Oscillator Granularity Error is:

$$\textit{DQS Oscillator Granularity Error} = \frac{2 * (0.4ns)}{100ns} = 0.8\%$$

This equates to a granularity timing error of 3.2ps.

Assuming a circuit Matching Error of 5.5ps across voltage and temperature, then the accuracy is:

$$\textit{DQS Oscillator Accuracy} = 1 - \frac{3.2 + 5.5}{400} = 97.7\%$$

Example: Running the DQS Oscillator for a longer period improves the accuracy. If the total time between start and stop commands is 250ns, and the maximum DQS clock tree delay is 400ps (tDQS2DQ max), then the DQS Oscillator Granularity Error is:

$$\textit{DQS Oscillator Granularity Error} = \frac{2 * (0.4ns)}{250ns} = 0.32\%$$

This equates to a granularity timing error or 1.28ps.

Assuming a circuit Matching Error of 5.5ps across voltage and temperature, then the accuracy is:

$$\textit{DQS Oscillator Accuracy} = 1 - \frac{2.56 + 5.5}{400} = 98.0\%$$

The result of the DQS Interval Oscillator is defined as the number of DQS Clock Tree Delays that can be counted within the “run time,” determined by the controller. The result is stored in MRXX-OP[X:X] and MRXX-OP[X:X]. MRXX contains the least significant bits (LSB) of the result, and MRXX contains the most significant bits (MSB) of the result. MRXX and MRXX are overwritten by the SDRAM when a MPC-1 [Stop DQS Osc] command is received. The SDRAM counter will count to its maximum value (=2^16) and stop. If the maximum value is read from the mode registers, then the memory controller must assume that the counter overflowed the register and discard the result. The longest “run time” for the oscillator that will not overflow the counter registers can be calculated as follows:

$$\textit{Longest Run Time Interval} = 2^{16} * tDQS2DQ(min)$$

The interval oscillator matching error is defined as the difference between the DQS training ckt(interval oscillator) and the actual DQS clock tree across voltage and temperature.

• Parameters:
  - tDQS2DQ: Actual DQS clock tree delay
  - tDQSOSC: Training ckt(interval oscillator) delay
  - OSCOffset: Average delay difference over voltage and temp
  - OSCMatch: DQS oscillator matching error

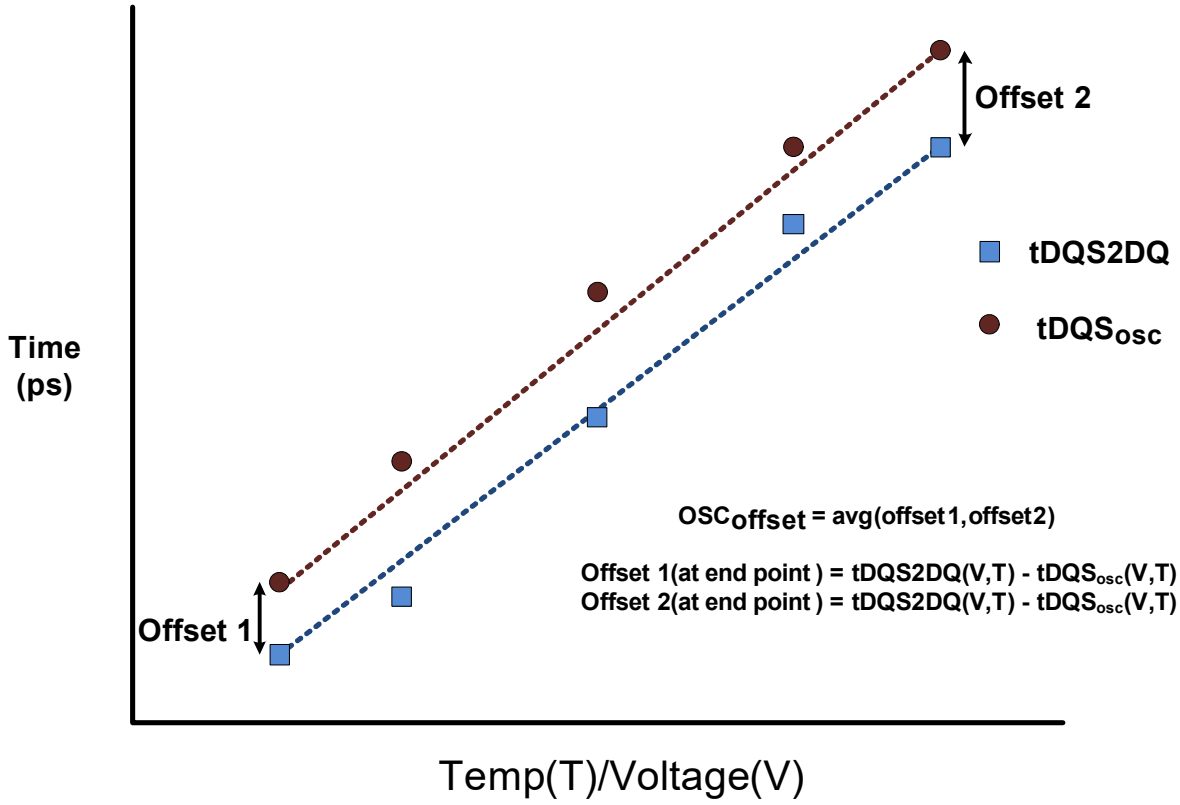


Figure 60 — Interval oscillator offset OSCoffset

• OSC_{Match} :

$$OSC_{Match} = [tDQS2DQ_{(V,T)} - tDQS_{OSC(V,T)} - OSC_{offset}]$$

• $tDQS_{OSC}$:

$$tDQS_{OSC(V,T)} = \frac{Runtime}{2 * Count}$$

Table 74 — DQS Oscillator Matching Error Specification

Parameter	Symbol	Min	Max	Units	Notes
DQS Oscillator Matching Error	OSC_{Match}	-10	+10	ps	1,2,3,4,5,6,7
DQS Oscillator Offset	OSC_{offset}	-100	100	ps	2,4,7

Note.

1. The OSC_{Match} is the matching error per between the actual DQS and DQS interval oscillator over voltage and temp.
2. This parameter will be characterized or guaranteed by design.
3. The OSC_{Match} is defined as the following:

$$OSC_{Match} = [tDQS2DQ_{(V,T)} - tDQS_{OSC(V,T)} - OSC_{offset}]$$

Where $tDQS2DQ_{(V,T)}$ and $tDQS_{OSC(V,T)}$ are determined over the same voltage and temp conditions.

4. The runtime of the oscillator must be at least 200ns for determining $tDQS_{OSC(V,T)}$

$$tDQS_{OSC(V,T)} = \frac{Runtime}{2 * Count}$$

5. The input stimulus for tDQS2DQ will be consistent over voltage and temp conditions.
6. The OSCoffset is the average difference of the endpoints across voltage and temp.
7. These parameters are defined per channel.
8. tDQS2DQ(V,T) delay will be the average of DQS to DQ delay over the runtime period.

The interval oscillator count read out timing

Table 75 — DQS Interval Oscillator Read out AC Timing

Parameter	Symbol	Min/Max	Value	Units	Notes
Delay time from OSC stop to Mode Register Readout	tOSCO	Min	tbd	ns	

4.26 2N Mode - Q4'16 Ballot #1830.47

2N mode allows the system to provide more setup and hold time on the CA bus. This mode can be enabled by MRx. DDR5 has defined two cycle commands, which requires the DRAM to capture the command differently between 1N and 2N modes. In both modes, the first half of the command is sample on the clock that the chip select is active. In 1N mode the second half of the command is sampled on the next clock edge. In 2N mode, the second half of the command is sampled 2 clocks after the first half. Non-target ODT signaling (on the chip select) is also delayed by a clock in 2N mode.

To the DRAM, one clock commands operate the same in 1N and 2N mode, with the command sampled on the same clock as the chip select active.

A 2 cycle or 1 cycle command can start on any clock (unlike geardown mode). Figure 61 below shows the differences between standard 1N mode with a 2 cycle read command, followed by a 1 cycle precharge command and it looks like when operated in 2N mode with the same commands. While in 2N mode, the host will never send two consecutive Chip Selects.

Table 76 — 2N Mode Register Config

MR Address	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TBD	Valid	Valid	Valid	Valid	Valid	Valid	Valid	2N_Mode

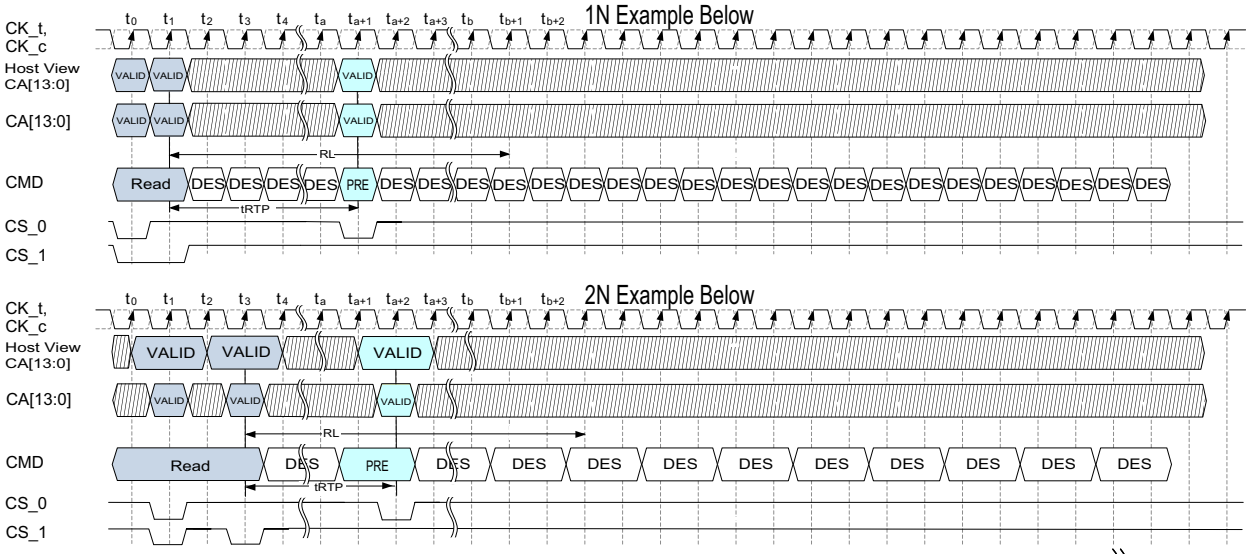
OP(0-7) can be programed with either "0" or "1".

Table 77 — 2N Mode Register Config

Function	Register Type	Operand	Data	Notes
2N_Mode	R/W	**OP[0]**	**0_B: 2N Mode (Default)** **1_B: 1N Mode**	**1**

1 - To ensure training modes can be enabled and run appropriately, the default (power-on) mode for DDR5 is 2N mode. Post CA Training, the user can configure this bit to put the device into either 1N mode or 2N mode. Both 1N and 2N modes are valid operating conditions for DDR5.

Figure 61 — Example of 1N vs 2N Mode - For reference only



NOTES : 1. The Host View CA[13:0] is shown for clarification, while CA[13:0] is what the DRAM should expect.
2. CS1 is shown for NT ODT clarification.
3. tRTP can be launched on odd or even clocks.

4.27 Fast Zero Mode - Q1'17 Ballot #1845.25 w/Editorial Updates

The DDR5 DRAM will support a mode that allows for an extremely quick way to flush the entire DRAM array with zeros. Normal expectation is that this function will be used during the configuration part of initialization, prior to most training.

The timing of this mode will be defined by tFastZero and will be bit density specific and will be done in a way as to not cause a power delivery concern. It will be initiated by a mode register bit that will automatically flip back to disabled once the operation has completed inside the DRAM. Since this operation will take several ms, it is proposed that this mode will utilize a mode register status flag set by the DRAM to indicate when the operation has completed.

The host will be responsible for monitoring this bit and will not resume normal traffic until after the DRAM has reported it as completed. It is the hosts responsibility to not issue more Fast Zero operations than the system PD can support.

Table 78 — tFastZero AC timing

Parameter	Symbol	Min/Max	8Gb	16Gb	32Gb	64Gb	Unit
Time required to complete Fast Zero mode	tFastZero	Max	30	60	110	TBD	ms

Table 79 — Fast Zero Mode Register

MR Address	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR49	Valid	Valid	Valid	Valid	Valid	Valid	Fast Zero Status	Fast Zero Entry

OP(0-7) can be programed with either "0" or "1".

Table 80 — Fast Zero Mode Register Details

Function	Register Type	Operand	Data	Notes
Fast Zero Entry	W	**OP[0]**	**0_B: Normal Operation (Default)** **1_B: Enter Fast Zero Mode**	
Fast Zero Status	R	**OP[1]**	**0_B: Complete** **1_B: In Progress**	**1**
RFU	TBD	**OP[7:2]**		

1 - This bit will stay as "1 - In Progress" until it has completed, upon which time it will revert back to "0 - Completed"

4.28 Write Pattern Command - Q4'16 Ballot #1830.48 w/Editorial Changes

Due to the significant percentage of writes that contain all zeros, this new mode is being proposed for inclusion into the DDR5 specification as a new WRITE Pattern command. When used effectively, the command can save power by not actually sending the data across the bus.

This new mode is operated very similar to a standard write command with the notable exceptions that it has it's own encoded WRITE Pattern command, no data is sent on the DQ bus, no toggling of DQS is needed, and the DRAM does not turn on any internal ODT. ECC code is assumed to be Zero for Write Pattern Command assuming the pattern was all Zeros.

Upon receiving the command, the DRAM device will source the input for the memory array from the Write Pattern Mode Registers instead of from the DQ bits themselves. The DQ mapping across the burst is shown below in DQ output mapping table. The host will not send any data during this time. All timing constraints are still measured from the clocks where the write command data would have been transfered. e.g. tWR is measured from end of write burst to PRE as shown below in Figure 62. The pattern used for this mode is enabled via a byte of mode registers. That pattern can be defaulted to all zeros, all ones, or something else, but can only be changed with a initialization. Changing this pattern can only be done via a MRW command. The power on default for this mode register is all zero's.

Table 81 — Write Pattern Mode Register

MR Address	WRITE Pattern	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR48	UI	Valid	Valid	Valid	Valid	Valid	Valid	Valid	Valid

NOTES:

1. OP[7:0] can be independently programmed with either "0" or "1".
2. Default is all zero's for OP[7:0]

The DQ output mapping for BL16 table below describes how the pattern stored in MR48 above will be mapped into the DRAM array across the DQ bits and Burst. The pattern is described as follows:

In the case of a x4 SDRAM device, only OP[3:0] will used, with each bit of the pattern corresponding to DQ[3:0] respectively. The same OP value will be repeated over the entire burst for that bit. (i.e. DQ0 store OP0 on every UI of the burst)

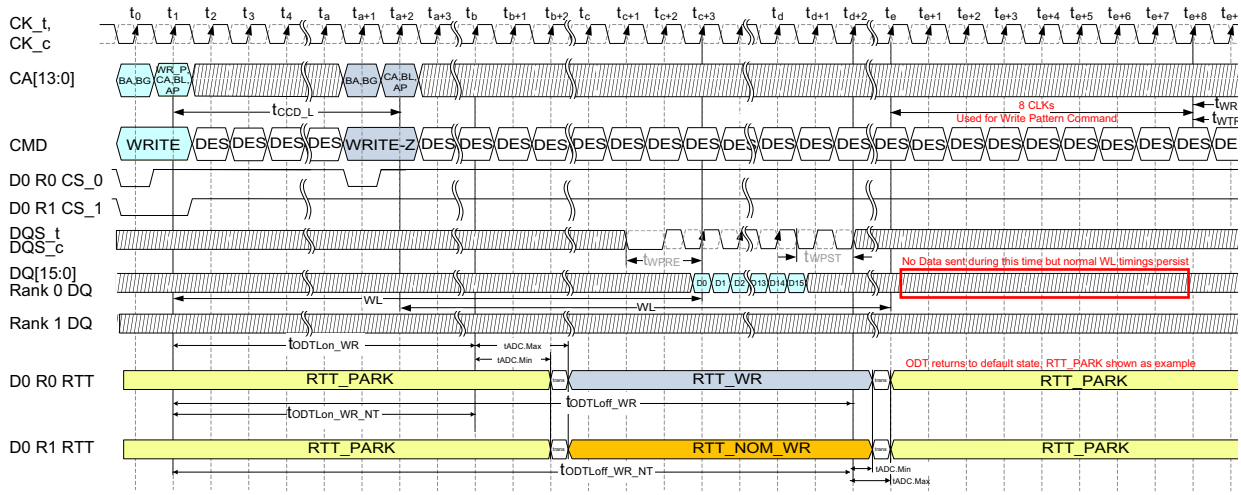
In the case of a x8 SDRAM device, the whole pattern OP[7:0] will be used, with each bit of the pattern corresponding to DQ[7:0] respectively. The same OP value will be repeated over the entire burst for that bit. (i.e. DQ0 store OP0 on every UI of the burst)

In the case of a x16 SDRAM device, the whole pattern OP[7:0] will be used, with each bit of the pattern corresponding to DQ[7:0] respectively and then that pattern will be repeated for DQ[8:15]. The same OP value will be repeated over the entire burst for that bit. (i.e. DQ0 store OP0 on every UI of the burst)

Table 37 - DQ output mapping for BL16

UI	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DQ0	OP0															
DQ1	OP1															
DQ2	OP2															
DQ3	OP3															
DQ4	OP4															
DQ5	OP5															
DQ6	OP6															
DQ7	OP7															
DQ8	OP0															
DQ9	OP1															
DQ10	OP2															
DQ11	OP3															
DQ12	OP4															
DQ13	OP5															
DQ14	OP6															
DQ15	OP7															
DMI0-1	INVALID															

Figure 62 — Example of Write Pattern Command



4.29 On-Die ECC - Q1'17 Ballot #1830.50

DDR5 devices will implement internal Single Error Correction (SEC) ECC to improve the data integrity within the DRAM. The DRAM will use 128 data bits to compute the ECC code of 8 ECC Check Bits. For the purpose of describing the ECC code, the 128 data bits are divided into four code word quarters - a top 64 bits (63:0) comprises Q1 and Q2. And a bottom 64 bits 127:64), Q3 and Q4 as shown in Table 82 and Table 83 respectively.

For a x4 DDR5 device, internal prefetch for on-die ECC is 128 bits even though a x4 is a 64 bit prefetch device. For each read or write transaction in a x4 device, an additional section of the DRAM array is accessed internally to provide the required additional 64 bits used in the 128 bit ECC computation. In other words, in an x4 device, each 8 bit ECC Check Bit word is tied to two 64 bit sections of the DRAM. In the case of a x8 device, no extra prefetch is required, as the prefetch is the same as the external transfer size. For an x16 device, two 128 bit data words and their corresponding 8 check bits are fetched from different banks. Each 128 Data bits and the corresponding 8 check bits bits are checked separately and in parallel.

On reads, the DRAM corrects any single bit errors before returning the data to the memory controller. The DRAM will not write the corrected data back to the array during a read cycle. For double bit errors, the ECC code (shown in Table 82 and Table 83) may miss correct a double bit the error into a triple bit error. This code will not alias any double bit error that occurs with one bit in Q1 and the other bit in Q2, likewise the code will not alias if the double bit error occurred with one error bit in Q3 and one error bit in Q4. The code may alias into a triple bit if a double bit error occurs in Q1 but the aliased bit will always occur in either the bottom half (Q3 or Q4). In the opposite case, if the double bit error occurs in for example Q3, the aliased bit will always occur in the top half of the code word (Q1 or Q2).

For a x 8 device, the top code word half is mapped to the first half of the 16 bit burst and the bottom code word half is mapped to the last half of the burst (Table 84). With this mapping, any 2 bit error that occurs in that might be aliased into a 3 bit error, the aliased third error would always show up in the other half of the access.

A x4 device has the Code Word into divided into two column accesses (N, N+y). The x4 code word is mapped similarly to the x8 mapping - the first half of the burst of DQ0-N, DQ1-N are mapped to Q1 and the second half of the burst to Q3. DQ2-N and DQ3-N are mapped to Q2 and Q4 for the first half of the burst and the second half respectively. The other half of the codeword in a x4 access is mapped as shown in Table 84.

On writes, the DRAM computes ECC and writes data and ECC bits to the array. If the external data transfer size is smaller than the 128 bit code word (x4 devices), then DRAM will have to perform an internal 'read-modify-write' operation. The DRAM will correct any single bit errors that result from the internal read before merging the incoming write data and then re-compute 8 ECC Check bits before writing data and ECC bits to the array. In the case of a x8 and x16 DDR5, no internal read is required.

For a x16 device, two 128 bit code words are read from two banks, one code word is mapped to DQ[0:7] and the other code word is mapped to DQ[8:15].

4.29.1 SEC Overview

The ECC blocks show in Figure 63 are the ECC Check Bit Generator, Syndrome Generator, Syndrome Decode and Correction. The Check Bit Generator and Syndrome Generator blocks are fully specified by the H matrix. This spec provides an example H matrix (Table 82 and Table 83) that maps errors as described above, as well as a sample XOR equation corresponding to the H matrix (Figure 4.29.2). Actual implementations in the DRAM may use a different H-Matrix as long as any double bit errors that are aliased into triple bits adhere to the mapping described above.

The Syndrome Decode block executes the following function:

Zero Syndrome => No Error

Non-Zero Syndrome matches one of the columns of the H matrix => Flip Corresponding bit (CE)

Non-Zero Syndrome that does not match any of the columns in the H matrix => DUE

CE: Corrected Error

DUE: Detected Uncorrected

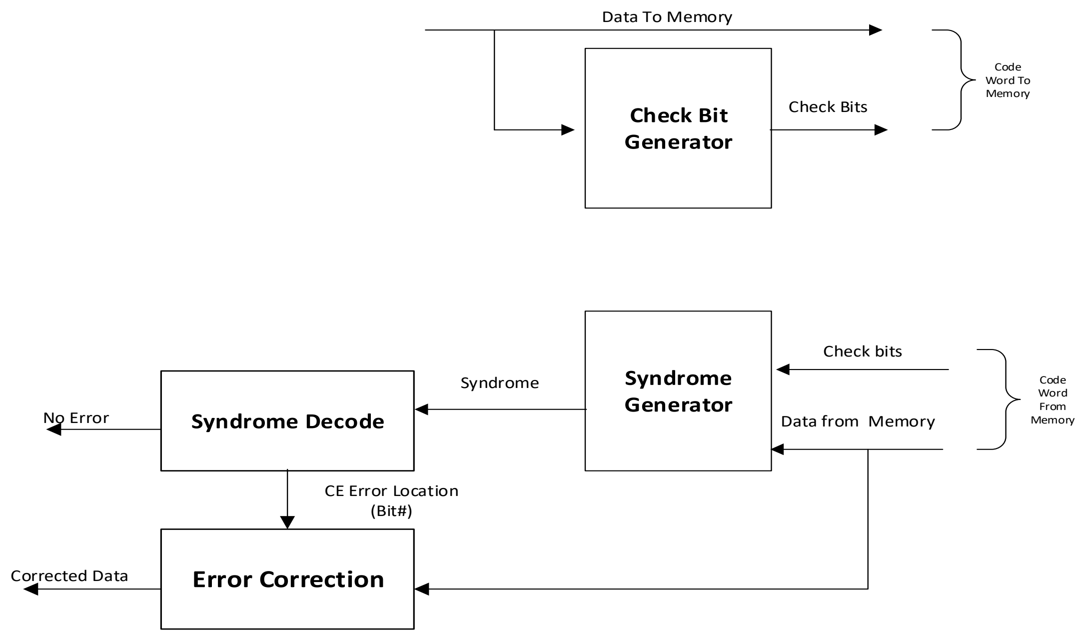


Figure 63 — On Die ECC Block Diagram

Table 82 — H Matrix for SEC Code - Top 64 bits, Q1, Q2

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CB0																	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
CB1																																
CB2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1																
CB3	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
CB4									1	1	1	1	1	1	1	1									1	1	1	1	1	1	1	1
CB5					1	1	1	1					1	1	1	1					1	1	1	1					1	1	1	1
CB6			1	1			1	1			1	1			1	1			1	1			1	1			1	1			1	1
CB7		1		1		1		1		1		1		1		1		1		1		1		1		1		1		1		1
	Q1																															

	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CB0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
CB1																	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
CB2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1																
CB3	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
CB4									1	1	1	1	1	1	1	1									1	1	1	1	1	1	1	1
CB5					1	1	1	1					1	1	1	1					1	1	1	1					1	1	1	1
CB6			1	1			1	1			1	1			1	1			1	1			1	1			1	1			1	1
CB7		1		1		1		1		1		1		1		1		1		1		1		1		1		1		1		1
	Q2																															

Table 83 — H-Matrix for SEC Code - Bottom 64 bits, Q3, Q4

	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
CB0																																
CB1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
CB2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1																
CB3																	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
CB4									1	1	1	1	1	1	1	1									1	1	1	1	1	1	1	1
CB5					1	1	1	1					1	1	1	1					1	1	1	1					1	1	1	1
CB6			1	1			1	1			1	1			1	1			1	1			1	1			1	1			1	1
CB7		1		1		1		1		1		1		1		1		1		1		1		1		1		1		1		1
	Q3																															

	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	20	121	122	123	124	125	126	127
CB0																	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
CB1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1																
CB2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
CB3	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1																
CB4									1	1	1	1	1	1	1	1									1	1	1	1	1	1	1	1
CB5					1	1	1	1					1	1	1	1					1	1	1	1					1	1	1	1
CB6			1	1			1	1			1	1			1	1			1	1			1	1			1	1			1	1
CB7		1		1		1		1		1		1		1		1		1		1		1		1		1		1		1		1
	Q4																															

4.29.2 Polynomial Code for H Matrix

CB0= XOR[16:63,112:127]
CB1 = XOR[48:111]
CB2 = XOR[0:15,32:47,64:79,96:127]
CB3 = XOR[0:63,80:111]
CB4 = XOR[8:15,24:31,40:47,56:63,72:79,88:95,104,111,120:127]
CB5 = XOR[4:7,12:15,20:23,28:31,36:39....116:119,124:127]
CB6 = XOR[2:3,6:7,14:15,18:19...122:123,126:127]
CB7 = XOR[1,3,5,7,9,11,13,.....123,125,127]

Table 84 — x4 x8 Burst Order and DQ Map vs Codeword

x4	DQ0-N	DQ1-N	DQ0-N+y	DQ1-N+y		DQ2-N	DQ3-N	DQ2-N+y	DQ3-N+y
x8	DQ0	DQ1	DQ2	DQ3		DQ4	DQ5	DQ6	DQ7
BL0	0	8	16	24		32	40	48	56
BL1	1	9	17	25		33	41	49	57
BL2	2	10	18	26		34	42	50	58
BL3	3	11	19	27		35	43	51	59
BL4	4	12	20	28		36	44	52	60
BL5	5	13	21	29		37	45	53	61
BL6	6	14	22	30		38	46	54	62
BL7	7	15	23	31		39	47	55	63
BL8	64	72	80	88		96	104	112	120
BL9	65	73	81	89		97	105	113	121
BL10	66	74	82	90		98	106	114	122
BL11	67	75	83	91		99	107	115	123
BL12	68	76	84	92		100	108	116	124
BL13	69	77	85	93		101	109	117	125
BL14	70	78	86	94		102	110	118	126
BL15	71	79	87	95		103	111	119	127

4.30 CRC - Q3'17 Ballot # 1830.05C

4.30.1 CRC polynomial and logic equation

DDR5 supports CRC for write and read operations. Write and read CRC can be enabled by separate mode register bits. Write CRC and data mask functions are not supported at the same time and cannot be enabled together.

The CRC polynomial used by DDR5 is the ATM-8 HEC, X^8+X^2+X^1+1 that is same as used on DDR4. A combinatorial logic block implementation of this 8-bit CRC for 64-bits of data contains TBD two-input XOR gates contained in eight 6 XOR gate deep trees.

The Table x shows error detection coverage of DDR5 CRC.

Table 85 — Error Detection Details

ERROR TYPE	DETECTION CAPABILITY
Random Single Bit Error	100%
Random Double Bit Error	100%
Random Odd Count Error	100%
Random Multi-Bit Error within Two adjacent Transfers	100%

CRC COMBINATORIAL LOGIC EQUATIONS

```
module CRC8_D64;
// polynomial: (0 1 2 8)
// data width: 64
// convention: the first serial data bit is D[63]
// initial condition all 0 implied
function [7:0]
nextCRC8_D64;
input [63:0] Data;
reg [63:0] D;
reg [7:0] NewCRC;
begin
D = Data
;
NewCRC[0] = D[63] ^ D[60] ^
D[56] ^ D[54] ^ D[53] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^
D[45] ^ D[43] ^ D[40] ^ D[39] ^ D[35] ^ D[34] ^ D[31] ^
D[30] ^ D[28] ^ D[23] ^ D[21] ^ D[19] ^ D[18] ^ D[16] ^
D[14] ^ D[12] ^ D[8] ^ D[7] ^ D[6] ^ D[0] ;
NewCRC[1] = D[63] ^ D[61] ^ D[60] ^ D[57] ^
D[56] ^ D[55] ^ D[52] ^ D[51] ^ D[48] ^ D[46] ^ D[45] ^
D[44] ^ D[43] ^ D[41] ^ D[39] ^ D[36] ^ D[34] ^ D[32] ^
D[30] ^ D[29] ^ D[28] ^ D[24] ^ D[23] ^ D[22] ^ D[21] ^
D[20] ^ D[18] ^ D[17] ^ D[16] ^ D[15] ^ D[14] ^ D[13] ^
D[12] ^ D[9] ^ D[6] ^ D[1] ^ D[0];
NewCRC[2] = D[63] ^ D[62] ^ D[61] ^ D[60] ^
D[58] ^ D[57] ^ D[54] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^
D[44] ^ D[43] ^ D[42] ^ D[39] ^ D[37] ^ D[34] ^ D[33] ^
D[29] ^ D[28] ^ D[25] ^ D[24] ^ D[22] ^ D[17] ^ D[15] ^
D[13] ^ D[12] ^ D[10] ^ D[8] ^ D[6] ^ D[2] ^ D[1] ^ D[0];
NewCRC[3] = D[63] ^ D[62] ^ D[61] ^ D[59] ^
D[58] ^ D[55] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^ D[45] ^
```

```
D[44] ^ D[43] ^ D[40] ^ D[38] ^ D[35] ^ D[34] ^ D[30] ^
D[29] ^ D[26] ^ D[25] ^ D[23] ^ D[18] ^ D[16] ^ D[14] ^
D[13] ^ D[11] ^ D[9] ^ D[7] ^ D[3] ^ D[2] ^ D[1];
NewCRC[4] = D[63] ^ D[62] ^ D[60] ^
D[59] ^ D[56] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^ D[46] ^
D[45] ^ D[44] ^ D[41] ^ D[39] ^ D[36] ^ D[35] ^ D[31] ^
D[30] ^ D[27] ^ D[26] ^ D[24] ^ D[19] ^ D[17] ^ D[15] ^
D[14] ^ D[12] ^ D[10] ^ D[8] ^ D[4] ^ D[3] ^ D[2];
NewCRC[5] = D[63] ^ D[61] ^ D[60] ^
D[57] ^ D[53] ^ D[51] ^ D[50] ^ D[49] ^ D[47] ^ D[46] ^
D[45] ^ D[42] ^ D[40] ^ D[37] ^ D[36] ^ D[32] ^ D[31] ^
D[28] ^ D[27] ^ D[25] ^ D[20] ^ D[18] ^ D[16] ^ D[15] ^
D[13] ^ D[11] ^ D[9] ^ D[5] ^ D[4] ^ D[3];
NewCRC[6] = D[62] ^ D[61] ^ D[58] ^
D[54] ^ D[52] ^ D[51] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^
D[43] ^ D[41] ^ D[38] ^ D[37] ^ D[33] ^ D[32] ^ D[29] ^
D[28] ^ D[26] ^ D[21] ^ D[19] ^ D[17] ^ D[16] ^ D[14] ^
D[12] ^ D[10] ^ D[6] ^ D[5] ^ D[4];
NewCRC[7] = D[63] ^ D[62] ^ D[59] ^
D[55] ^ D[53] ^ D[52] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^
D[44] ^ D[42] ^ D[39] ^ D[38] ^ D[34] ^ D[33] ^ D[30] ^
D[29] ^ D[27] ^ D[22] ^ D[20] ^ D[18] ^ D[17] ^ D[15] ^
D[13] ^ D[11] ^ D[7] ^ D[6] ^ D[5];
nextCRC8_D64 = NewCRC;
```

4.30.2 CRC data bit mapping for x4 devices

The following figure shows detailed bit mapping for a x4 device. This bit mapping is common between write and read CRC operations.

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7

Figure 64 — CRC bit mapping for x4 device

4.30.3 CRC data bit mapping for x8 devices

The following figure shows detailed bit mapping for a x8 device. This bit mapping is common between write and read CRC operations. x8 devices have two DQ nibbles and each DQ nibble has its own eight CRC bits to protect 64 data bits. Therefore, a x8 device will have two identical CRC trees implemented.

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7
DQ4	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ5	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ6	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ7	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7

Figure 65 — CRC bit mapping for x8 device

4.30.4 CRC data bit mapping for x16 devices

The following figure shows detailed bit mapping for a x16 device. This bit mapping is common between write and read CRC operations. x16 devices have four DQ nibbles and each DQ nibble has its own eight CRC bits to protect 64 data bits. Therefore, a x16 device will have four identical CRC trees implemented.

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7
DQ4	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ5	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ6	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ7	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7
DQ8	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ9	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ10	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ11	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7
DQ12	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ13	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ14	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ15	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7

Figure 66 — CRC bit mapping for x16 device

4.30.5 Write CRC for x4, x8 and x16 devices

The controller generates the CRC checksum and forms the write data frames as shown in <Link>Chapter 4.30.2 to <Link>Chapter 4.30.4.

Write CRC function can be enabled or disabled per each nibble independently in x8 device. There are two separate write CRC enable MR bits (for upper and lower nibbles) defined for x8. When at least one of two write CRC enable bits is set to '1' in x8, the timings of write CRC enable mode is applied to the entire device (i.e. both nibbles). When write CRC is enable in one nibble and disabled in the other nibble in x8, then the DRAM does not check CRC errors on the disabled nibble, and hence the ALERT_n signal and any internal status bit related to CRC error is not impacted by the disabled nibble.

In case of x4 or x16, only one of two write CRC enable bit is used as defined in the MR table (figure TBD). The unused write CRC enable bit is don't care in x4 and x16.

The DRAM checks for an error in received code words per each write CRC enabled nibble by comparing the received checksum against the computed checksum and reports errors using the ALERT_n signal if there is a mis-match in any of nibbles.

DRAM can write data to the DRAM core without waiting for CRC check for full writes. If bad data is written to the DRAM core then controller will retry the transaction and overwrite the bad data. Controller is responsible for data coherency.

There is no write latency adder when write CRC is enabled.

4.30.6 Write CRC auto-disable

CRC auto-disable mode is enabled by programming the CRC auto-disable mode enable bit to '1'. When this mode is enabled, DRAM counts the number of CRC error occurrence per chip (one counter per chip for x4, x8 and x16). When the number of CRC errors exceeds the CRC threshold (between 0 and 127) as programmed in MR51[6:0] since the counter was reset last time, then DRAM disables write CRC checking of all nibbles and sets the CRC auto-disable status bit to '1'. If DRAM was already driving ALERT_n to low due to current or previous CRC error then it may release it, but CRC_ALERT_PW_min should be still satisfied. The counter is reset after the predetermined number of writes (between 0 and 127; 0 means infinite window) as programmed in MR52[6:0] so that the error count would be accumulated only in between counter resets. However, once CRC checking was disabled because the CRC error count exceeded the CRC threshold, write CRC checking is not re-enabled even if the error count is below the threshold in between counter resets in any later time. Write CRC checking can be re-enabled by resetting the CRC auto-disable status bit to '0'.

4.30.7 Read CRC for x4, x8 and x16 devices

The DRAM generates the CRC checksum and forms the read data frames as shown in <Link>Chapter 4.30.2 to <Link>Chapter 4.30.4. The controller can check for an error in received code words per nibble by comparing the received checksum against the computed checksum and if there is a mis-match in any of nibbles then controller may retry the transaction.

When read CRC is enabled, DRAM's CRC generator overrides C3 and C2 to '00' ~~in case of BL16 and C2 to '0' in case of BC8~~, and CRC bits are calculated based on the sequential burst order ('0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F' in BL16, '0,1,2,3,4,5,6,7,T,T,T,T,T,T,T,T' or 'T,T,T,T,T,T,T,T,8,9,A,B,C,D,E,F' in BC8) of the read data. The override values do not modify the actual data burst ordering, and are only used for the CRC calculations. Actual data burst follows the burst order as indicated by C3 and C2 in the read command.

Read latency adder is TBD when read CRC is enabled.

4.30.8 Write CRC error handling

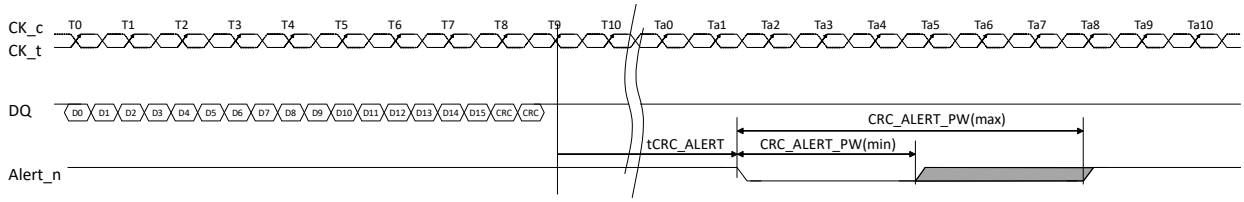
When DRAM detects CRC error on received code words in any of nibbles, then it drives ALERT_n signal to ‘0’ for TBD clocks.

The latency to ALERT_n signal is defined as tCRC_ALERT in the figure below.

DRAM will set Write CRC Error Status bit in A[3] of MR50 to '1' ~~and CRC Error Status bit in MR_TBD to '1'~~ upon detecting a CRC error. The Write CRC Error Status bit remains set at '1' until the host clears it explicitly using an MRW command.

The controller upon seeing an error as a pulse width will retry the write transactions. The controller understands the worst case delay for ALERT_n (during init) and can backup the transactions accordingly or the controller can be made more intelligent and try to correlate the write CRC error to a specific rank or a transaction. The controller is also responsible for opening any pages and ensuring that retrying of writes is done in a coherent fashion.

The pulse width may be seen longer than TBD clocks at the controller if there are multiple CRC errors as the ALERT_n is a daisy chain bus.



NOTE 1. CRC_ALERT_PW is specified from the point where the DRAM starts to drive the signal low to the point where the DRAM driver releases and the controller starts to pull the signal up.
NOTE 2. Timing diagram applies to x4, x8 and x16 devices.

Figure 67 — CRC Error Reporting Timing diagram

Table 86 — CRC Error Handling Timing Parameters

Symbol	Description	min	max	unit
tCRC_ALERT	CRC Alert Delay Time	TBD	TBD	ns
CRC_ALERT_PW	CRC Alert Pulse Width	TBD	TBD	UI

4.30.9 CRC bit mapping in BC8 mode

CRC bits are always transferred on 17th and 18th UI, in BC8 mode. When read CRC is enabled during BC8 read, DQ bits are driven high and DQS is toggled by DRAM during the chopped data bursts. When write CRC is enabled during BC8 write, DQ bits must be driven high and DQS must be toggled by controller during the chopped data bursts. In BC8 mode, read CRC and write CRC bits are calculated with the inputs to the CRC engine for the chopped data bursts replaced by all '1's.

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7

Figure 68 — CRC bit mapping in BC8 modes for x4 device

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7
DQ4	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ5	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ6	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ7	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7

Figure 69 — CRC bit mapping in BC8 modes for x8 device

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7
DQ4	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ5	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ6	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ7	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7
DQ8	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ9	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ10	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ11	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7
DQ12	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ13	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ14	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ15	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7

Figure 70 — CRC bit mapping in BC8 modes for x16 device

4.30.10 CRC bit mapping in BL32 mode

In BL32 mode, CRC bits are separately calculated for the first half and the second half of the data. CRC bits for the first half of the data are transferred on 17th and 18th UI, and CRC bits for the second half of the data are transferred on 35th and 36th UI.

4.31 Loopback - Q3'17 Ballot #1830.92A

With Loopback, DDR5 can feed a received signal or data back out to an external receiver for multiple purposes. Loopback allows the host (memory controller or test instrument) to immediately read back data that was just sent to the DRAM without having to issue multiple WRITE/READ commands. Loopback in DDR5 DRAM requires that the data be sent to the Loopback path before sending it to the core so no READ/WRTE commands are required for Loopback to be operational. There are also inherent limitations when characterizing the receiver using statistical analysis methods such as Bit Error Rate (BER) analysis. At BER=$1E^{-16}$, for example, (1) there is not enough memory depth in the DRAM to store all the $1E^{-16}$ data; (2) the amount of time to perform multiple WRITE/READ commands to/from the memory is prohibitively long; (3) since the amount of time involved performing these operations is much longer than the DRAM refresh rate interval, the host or memory controller must also manage Refreshes during testing to ensure data retention; and (4) limited pattern depth means limited Inter Symbol Interference (ISI) and limited Random Jitter (Rj), and, therefore, limited errors at the receiver. Use of the Loopback feature is a necessity for characterizing the receiver without the limitations and complexities of other traditional validation methods. Loopback can also be used during "normal" operation, i.e., during training and when an operating system is loaded. The methodology for such will be provided in future ballot.

4.31.1 Components of the Loopback

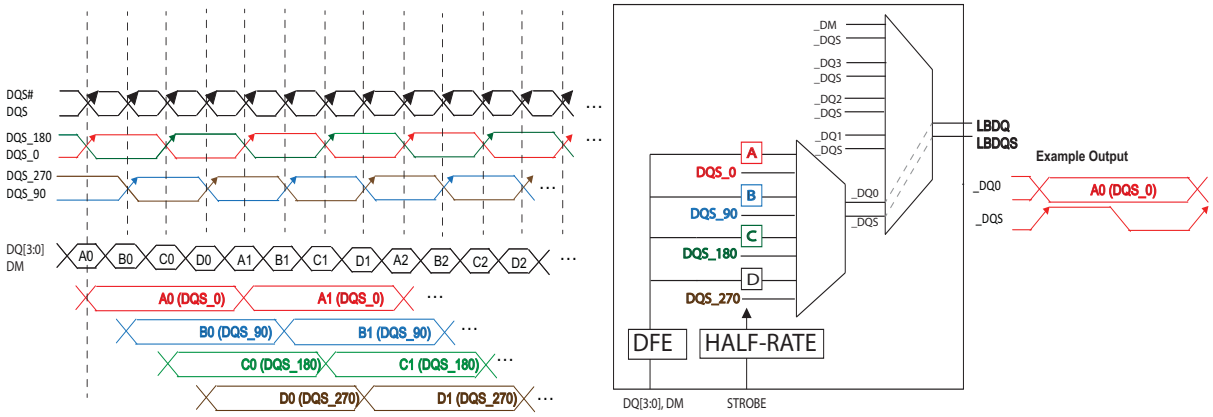
The Loopback requires 2 output pins (one single-ended Loopback strobe LBDQS and one single-ended Loopback data LBDQ). The Loopback may also consist of multiplexers to select the DQ and Phase for Loopback.

Pin assignment location for Loopback pins on x4/x8 are defined as A9 for LBDQS and A1 for LBDQ. Pin assignment location for Loopback pins on x16 is TBD.

The AC/DC timing, levels and electrical package specifications for the Loopback pins are TBD.

Figure 71 shows an example of a Loopback implementation for 4-way interleave X4 DRAM. This example requires a divided clock to produce DQS_0, DQS_90, DQS_180 and DQS_270. Phase A through D refers to the 4-bit naturally aligned bits in a data stream. The output of the DQ slicer runs at 1/4 the speed as received data. In a 4-way interleave design, the data is received at full speed, but internally the data is latched only at quarter speed. For example, if the input bit stream is consist of A, B, C, D, then the multiplexer input "A" receives data bit A and strobe DQS_0; multiplexer input "B" receives data bit B and strobe DQS_90; multiplexer input "C" receives data bit C and strobe DQS_180; and multiplexer input "D" receives data bit D and DQS_270.

Figure 71 — Example of 4-Way Interleave Loopback Circuit on a X4 SDRAM



5 On-Die Termination

5.1 On-Die Termination for DQ - Q4'16 Ballot #1830.45

ODT (On-Die Termination) is a feature of the DDR5 SDRAM that allows the DRAM to change termination resistance for each DQ, Unlike previous DDR technologies, DDR5 no longer has a physical ODT pin and all ODT based control is now command & mode register based. DQS_t, DQS_c and DM_n for x4 and x8 conjuration (and TDQS_t, TDQS_c for X8 conjuration), when enabled via MR=TBD via Read (for NT ODT usage), Write Commands or Default Parking value with MR setting. For x16 configuration, ODT is applied to each DQU, DQL, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n and DML_n signal. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently change termination resistance for any or all DRAM devices. In addition to the control capability of the DQ ODT, independent timing support of the DQS ODT is also provided (though the same RTT will be used). This addition allows for adjusting the delay common in an unmatched architecture. DQS RTT offset control mode is enabled via a Mode Register.

The ODT feature is turned off and not supported in Self-Refresh mode, but does have an optional mode with in Power Down. A simple functional representation of the DRAM ODT feature is shown in Figure 72.

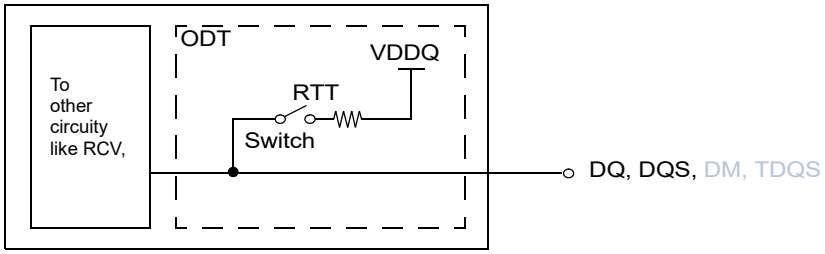


Figure 72 — Functional Representation of ODT

The switch is enabled by the internal ODT control logic, which uses command decode, Mode Register Settings and other control information, see below. The value of RTT is determined by the settings of Mode Register bits (see Section TBD).

5.2 ODT Modes, Timing Diagrams and State Table

The ODT Mode of DDR5 SDRAM has 5 states,, Data Termination Disable, RTT_WR, RTT_NOM_RD, RTT_NOM_WR and RTT_PARK. The ODT Mode is enabled based on Mode Registers TBD. In this case, the value of RTT is determined by the settings of those bits.

After entering Self-Refresh mode, DRAM automatically disables ODT termination and set Hi-Z as termination state regardless of these setting.

Application: Controller can control each RTT condition with WR/RD command and use of ODT Offset Control Mode Registers.

- RTT_WR: The rank that is being written to provide termination and adjusts timing based on ODT Control Mode Register settings.
- RTT_NOM_RD: DRAM turns ON RTT_NOM_RD if it sees CS asserted during the second pulse of the READ command (except when ODT is disabled by MR31).
- RTT_NOM_WR: DRAM turns ON RTT_NOM_WR if it sees a CS asserted during the second pulse of the WRITE command (except when ODT is disabled by MR31)
- RTT_PARK: Default parked value set via MR30 to be enabled when a READ or WRITE is not active.
- Data Termination Disable: DRAM driving data upon receiving READ command disables the termination after RL-X and stays off for a duration of BL/2 + X clock cycles. X is dependent on the preamble and is TBD.

Those RTT values have priority as following.
1. Data Termination Disable
2. RTT_WR
3. RTT_NOM_RD
4. RTT_NOM_WR
4. RTT_PARK

which means if there is WRITE command, then DRAM turns on RTT_WR not RTT_NOM_WR or RTT_NOM_RD, and also if there is READ command, then DRAM disables data termination and goes into Driving mode. If during the second pulse of a READ or WRITE command, a CS enable is sent, then Non-Target ODT is enabled and the appropriate RTT_NOM_RD or RTT_NOM_WR is enabled for the non-target rank. This provides additional and potentially different term options for the other ranks on the channel.

Table 87 — Termination State Table

Command	Mode Register Configuration Settings				Results		Note
	RTT_PARK	RTT_WR	RTT_NOM_WR	RTT_NOM_RD	Target DRAM Term	Non-Target DRAM Term	
ANY	Disabled				HI-Z (ODT OFF)		3
Any Non-Term CMD	Enabled	Don't Care			RTT_PARK	RTT_PARK	4
WR/MRW*	Disabled			Don't Care	HI-Z (ODT OFF)	HI-Z (ODT OFF)	6
	Disabled		Enabled		HI-Z (ODT OFF)	RTT_NOM_WR	6
	Disabled	Enabled	Disabled		RTT_WR	HI-Z (ODT OFF)	6
	Don't Care	Enabled			RTT_WR	RTT_NOM_WR	2,6
	Enabled		Disabled		RTT_WR	HI-Z (ODT OFF)	2,5,6
	Enabled	Disabled	Enabled		RTT_PARK	RTT_NOM_WR	6
	Enabled	Disabled			RTT_PARK	HI-Z (ODT OFF)	5,6
RD/MRR	Enabled	Don't Care		Disabled	HI-Z (ODT OFF)	HI-Z (ODT OFF)	1,5
	Don't Care			Enabled	HI-Z (ODT OFF)	RTT_NOM_RD	1

NOTE 1 - When read command is executed, DRAM termination state of target rank will be Hi-Z for defined period independent of MR setting of RTT_PARK/RTT_NOM_RD/ RTT_NOM_WR.
NOTE 2 - If RTT_WR is enabled, RTT_WR will be activated by Write command for defined period time independent of MR setting of RTT_PARK /RTT_NOM.
NOTE 3 - If all RTT configs are disabled, ODT receiver power will be turned off to save power.
NOTE 4 - If RTT_PARK is enabled, DRAM RTT_PARK termination will be enabled while WR/MRW*/RD/MRR are not being executed.
NOTE 5 - When a Non-Target ODT command is executed and the RTT_NOM_WR or RTT_NOM_RD is disabled, the DRAM termination state of the non-target rank will be Hi-Z for a defined period, independent of the MR setting of RTT_PARK.
NOTE 6 - MRW* refers to only MRW commands while in PDA mode.

.

On-Die Termination effective resistance RTT is defined by MR bits.
ODT is applied to the DQ, DM, DQS_T/DQS_C and TDQS_T/TDQS_C (x8 devices only) pins.
A functional representation of the on-die termination is shown in the figure below.

$$RTT = \frac{VDDQ - Vout}{|\ I\ out\ |}$$

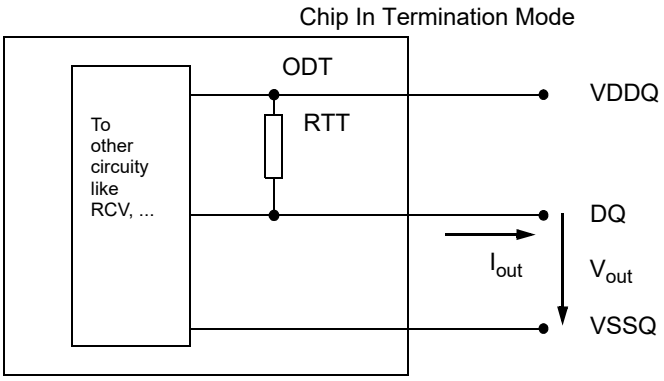


Figure 73 — On Die Termination

On die termination effective Rtt values supported are 240,120, 80, 60, 48, 40, 34 ohms.

Table 88 — ODT Electrical Characteristics RZQ=240Ω +/-1% entire temperature operation range; after proper ZQ calibration

RTT	Vout	Min	Nom	Max	Unit	NOTE
240Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ	1,2,3
	VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ	1,2,3
120Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/2	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/2	1,2,3
	VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/2	1,2,3
80Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/3	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/3	1,2,3
	VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/3	1,2,3
60Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/4	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/4	1,2,3
	VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/4	1,2,3
48Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/5	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2,3
	VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/5	1,2,3
40Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/6	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/6	1,2,3
	VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/6	1,2,3
34Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2,3
	VOHdc= 0.95* VDDQ	0.8	1	1.1	RZQ/7	1,2,3
DQ-DQ Mismatch within byte	VOMdc = 0.8* VDDQ	0	-	10	%	1,2,4,5,6

NOTES:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. Pull-up ODT resistors are recommended to be calibrated at 0.8*VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5*VDDQ and 0.95*VDDQ.
3. The tolerance limits are specified under the condition that VDDQ=VDD and VSSQ=VSS
4. DQ to DQ mismatch within byte variation for a given component including DQS_T and DQS_C (characterized)
5. RTT variance range ratio to RTT Nominal value in a given component, including DQS_t and DQS_c.

$$\text{DQ-DQ Mismatch in a Device} = \frac{\text{RTTMax -RTTMin}}{\text{RTTNOM}} * 100$$

6. This parameter of x16 device is specified for Upper byte and Lower byte.

5.3 Dynamic ODT

In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR5 SDRAM can be changed without issuing an MRW command. This requirement is supported by the “Dynamic ODT” feature as described as follows:

5.3.1 ODT Functional Description

The Dynamic ODT Mode is enabled if bit x of MR2 is set to ’1’. The function is described as follows:

• Four RTT values are available: RTT_NOM_RD, RTT_NOM_WR, RTT_PARK and RTT_WR.
- The value for RTT_NOM_RD is preselected via OP[5:3] in MR3
- The value for RTT_NOM_WR is preselected via OP[2:0] in MR3
- The value for RTT_WR is preselected via OP[5:3] in MR2
- The value for RTT_PARK is preselected via OP[2:0] in MR2

• During operation without commands, the termination is controlled as follows;
- Nominal termination strength for all types (RTT_NOM_RD, RTT_NOM_WR, RTT_WR & RTT_PARK) are selected.
- RTT_NOM_RD & RTT_NOM_WR on/off timings are controlled via the respective NT Read and Write command and latencies.

• When a write command (WR) is registered, the termination is controlled as follows:
- A latency ODTLon_WR after the write command, termination strength RTT_WR is selected.
- A latency ODTLoff_WR after the write command, termination strength RTT_WR is de-selected.

Table 89 — Latencies and timing parameters relevant for Dynamic ODT with 1tCK preamble mode and CRC disabled

Name and Description	Abbr.	Defined from	Define to	Definition for all DDR5 speed bins	Unit
ODT Latency On from WRITE command to RTT Enable	ODTLon_WR	Registering external write command	Change RTT strength from Previous State to RTT_WR	ODTLon_WL = WL - 2	nCK
ODT Latency On from NT WRITE command to RTT Enable	ODTLoff_WR_NT	Registering external write command	Change RTT strength from Previous State to RTT_NOM_WR	ODTLon_WR_NT = ODTLon_WR	
ODT Latency Off from WRITE command to RTT Disable	ODTLoff_WR	Registering external write command	Change RTT strength from RTT_WR to RTT_PARK/ RTT_NOM_RD/ RTT_NOM_WR/ Hi-Z	ODTLoff_WR = TBD	nCK
ODT Latency Off from NT WRITE command to RTT Disable	ODTLoff_WR_NT	Registering external write command	Change RTT strength from RTT_NOM_WR to RTT_PARK/ RTT_NOM_RD/ RTT_WR/ Hi-Z	ODTLoff_WR_NT = ODTLoff_WR	
ODT Latency On from READ command to RTT Enable	ODTLon_RD	Registering external read command	Change RTT strength from Previous State to Hi-Z	ODTLon_RD = TBD	nCK
ODT Latency On from NT READ command to RTT Enable	ODTLoff_RD_NT	Registering external read command	Change RTT strength from Previous State to RTT_NOM_RD	ODTLoff_RD_NT = ODTLon_RD	
ODT Latency Off from READ command to RTT Disable	ODTLoff_RD	Registering external read command	Change RTT strength from Hi-Z to RTT_PARK/ RTT_NOM_RD/ RTT_NOM_WR/ RTT_WR	ODTLoff_RD=TBD	nCK
ODT Latency Off from NT READ command to RTT Disable	ODTLoff_RD_NT	Registering external read command	Change RTT strength from RTT_NOM_RD to RTT_PARK/ RTT_NOM_WR/ RTT_WR/ HI-Z	ODTLoff_RD_NT = ODTLoff_RD	
RTT change skew	tADC	Transitioning from one RTT State to the next RTT State	RTT valid	tADC(min) = 150 tADC(max) = 450	ps

5.3.2 ODT Timing Diagrams

The following pages provide examples of ODT utilization timing diagrams. Examples of write to write, read to write and read to read are provided for clarification only. Implementations may vary, including termination on other DIMMS.

It is the controllers responsibility to manage command spacing and the programmable aspect of tODLon/off times to ensure that preambles and postambles are included in the RTT ON time. Conflicts on RTT ON times need to be discussed.

All timings noted in the figures below are just used as reference and are subject to change when the parameters are defined.

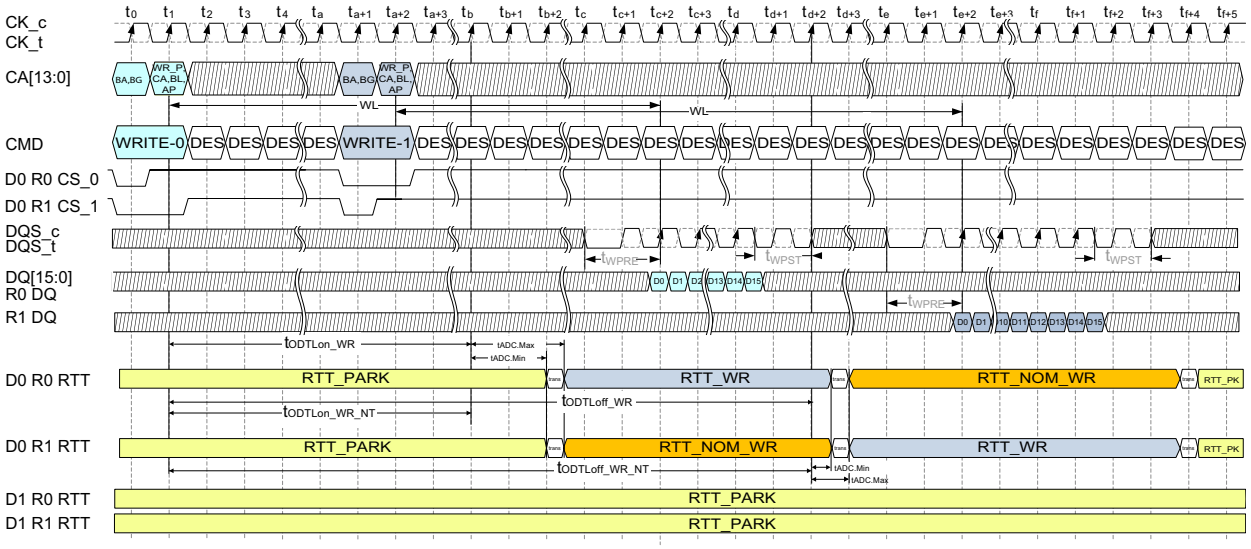


Figure 74 — Example of Write to Write turn around, Different Ranks

NOTES:
1. ODTLon_WR, ODTLon_WR_NT, ODTLoff_WR and ODTLoff_WR_NT are based on MRxx settings that can push out or pull in the RTT enable and disable time.
2. DO & D1 indicate DIMM Slot 0 and Slot 1 respectively and R0 & R1 indicate Rank 0 and Rank 1 respectively. For reference only.

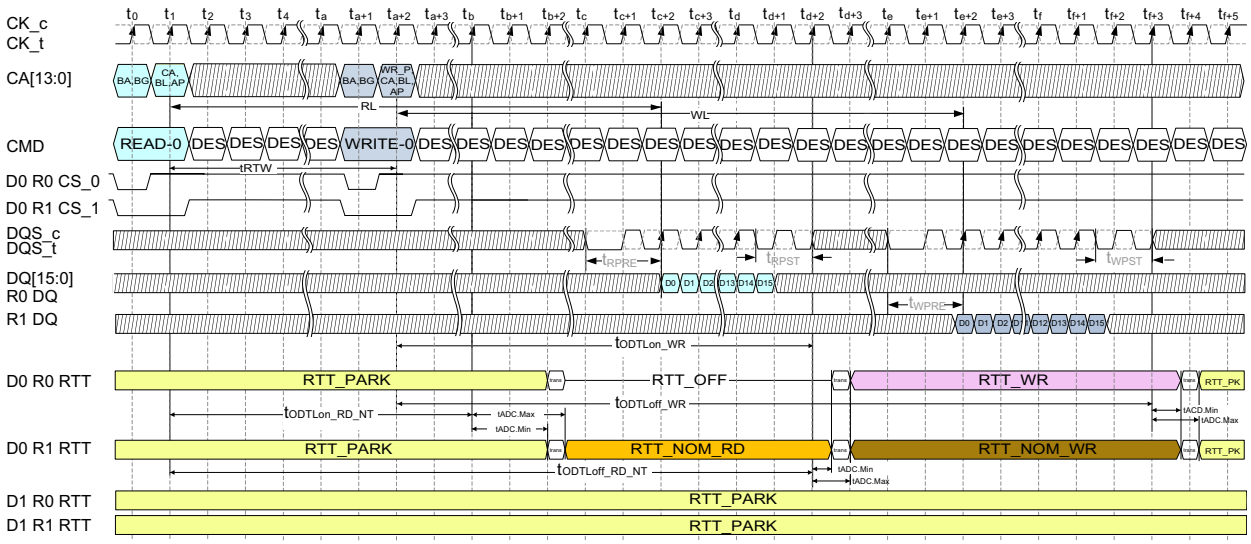


Figure 75 — Example of Read to Write turn around, Different Ranks

NOTES:
1. ODTLon_WR, ODTLon_WR_NT, ODTLoff_WR and ODTLoff_WR_NT are based on MRxx settings that can push out or pull in the RTT enable and disable time.
2. ODTLon_RD, ODTLon_RD_NT, ODTLoff_RD and ODTLoff_RD_NT are based on MRxx settings that can push out or pull in the RTT enable and disable time.
3. DO & D1 indicate DIMM Slot 0 and Slot 1 respectively and R0 & R1 indicate Rank 0 and Rank 1 respectively. For reference only.

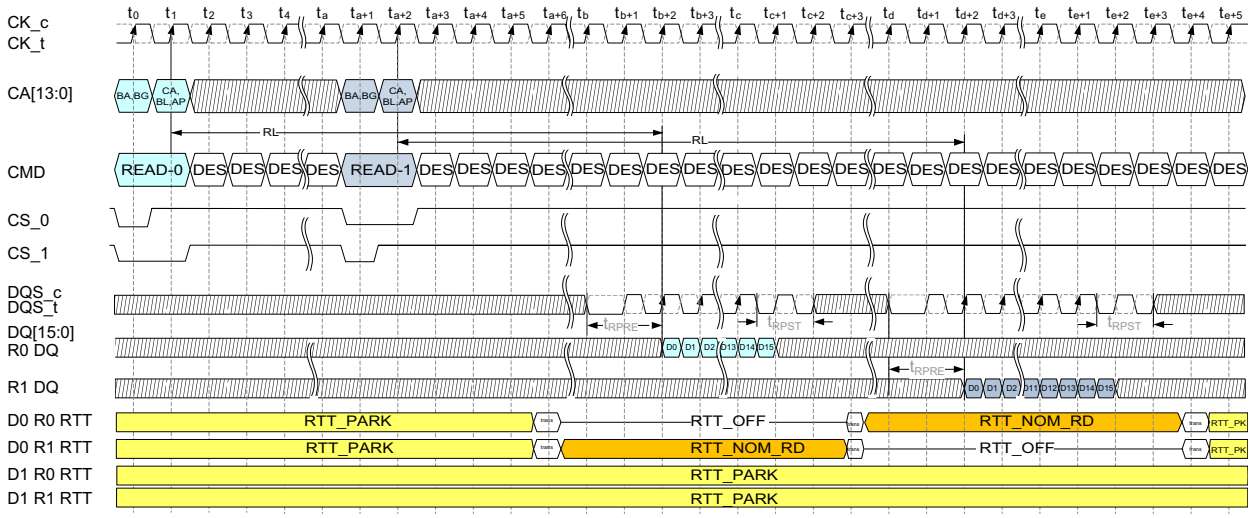


Figure 76 — Example of Read to Read turn around, Different Ranks

NOTES:
1. ODTLon_RD, ODTLon_RD_NT, ODTLoff_RD and ODTLoff_RD_NT are based on MRxx settings that can push out or pull in the RTT enable and disable time.
3. DO & D1 indicate DIMM Slot 0 and Slot 1 respectively and R0 & R1 indicate Rank 0 and Rank 1 respectively. For reference only.

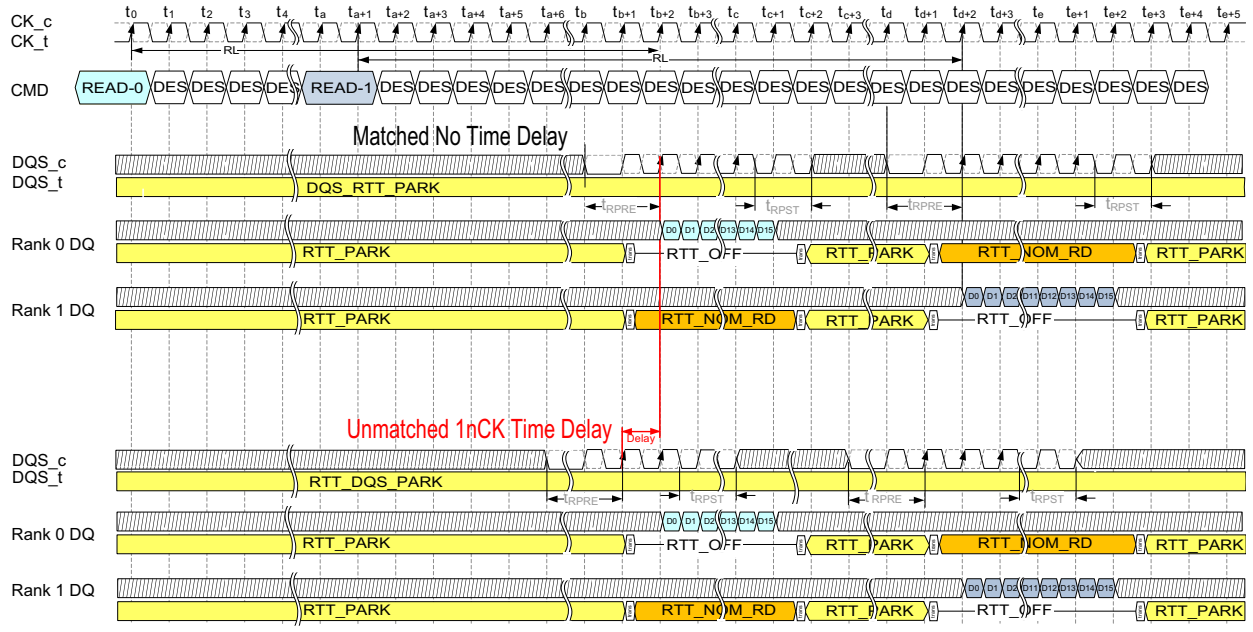


Figure 77 — Example of Unmatched Architecture where DQS RTT is shifted independent of DQ RTT

This diagram depicts an example where an unmatched receiver could have up to a 1nCK delay between when it gets the DQS and the DATA. In this example, we would want to enable the RTT_DQS_NOM_RD 1nCK earlier that in a typical matched case. The 1nCK is shown as the red delay in the lower part of the diagram. Delay is not meant as a new parameter but just graphically shows how the DQS RTT offset could be different than the DQ. The ODTLon_DQS_RD_NT and the ODTLoff_DQS_RD_NT parameters would control the delay.

NOTES:
1. ODTLon_DQS_RD, ODTLon_DQS_RD_NT, ODTLoff_DQS_RD and ODTLoff_DQS_RD_NT are based on MRxx settings that can push out or pull in the DQS RTT enable and disable time. Not all parameters are shown but they follow the traditional ODTLon/off timings.

5.4 On-Die Termination for CA - Q2'16 Ballot #1830.73A w/Editorial Updates

The DDR5 DRAM includes CA ODT (On-Die Termination) termination resistance for CK_t, CK_c, CS and CA signals.

The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for any target DRAM devices via MR setting.

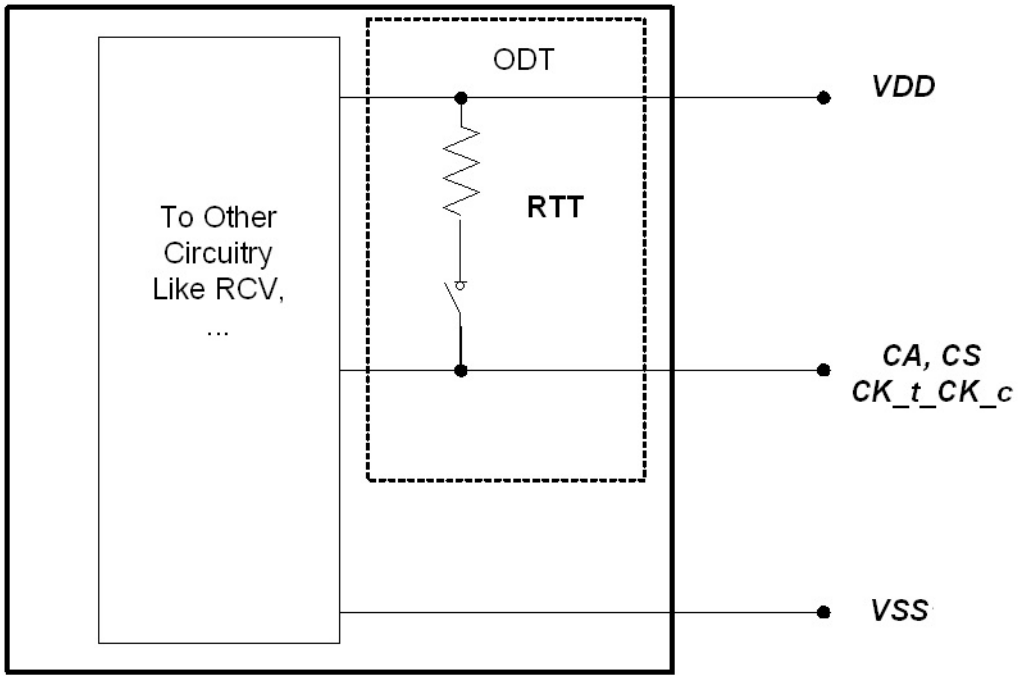


Figure 78 — A simple functional representation of the DRAM CA ODT feature

The ODT termination resistance during power up will be set to the default values based on MR32 and MR33. The ODT resistance values can be configured by those same registers.

The CA ODT of the device is designed to enable one more ranks to terminate the entire command bus in a multi-rank system. For this reason, the CA ODT remains on even when the device is in the power-down or self-refresh power-down states.

On-Die Termination effective resistance RTT is define by MRS bits.
ODT is applied to CK_t,CK_c, CS and CA pins

$$RTT = \frac{VDD\text{-}Vout}{|\ I\ out\ |}$$

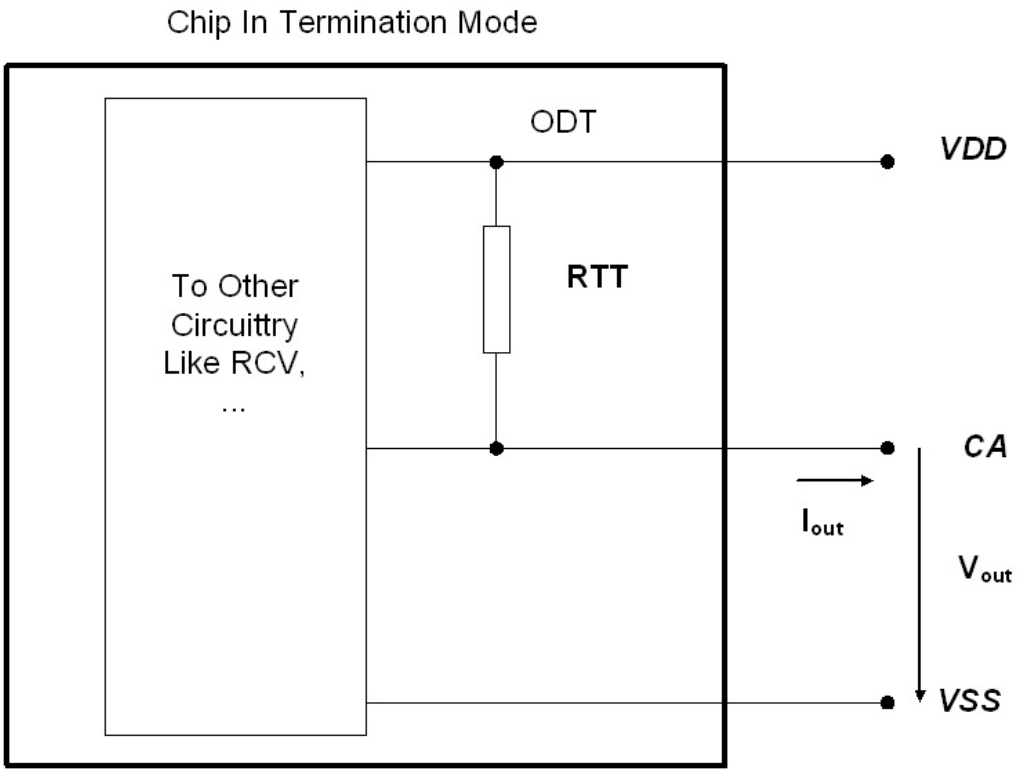


Figure 79 — A functional representation of the on-die termination

5.4.1 Supported On Die Termination Values

On die termination effective Rtt values supported are 480, 240, 80, 60, 40 ohms

Table 1 - ODT Electrical Characteristics RZQ=240Ω +/-1% entire temperature operation range; after proper ZQ calibration; VDD=VDDQ

MR	RTT	Vout	Min	Nom	Max	Unit	Note
MR32 for CK MR33 for CA & CS	480Ω	V_{OLdc}= 0.5* VDD	0.7	1	1.4	R_{ZQ}*2	1,2,3
		V_{OMdc}= 0.8* VDD	0.7	1	1.3	R_{ZQ}*2	1,2,3
		V_{OHdc}= 0.95* VDD	0.6	1	1.3	R_{ZQ}*2	1,2,3
MR32 for CK MR33 for CA & CS	240Ω	V_{OLdc}= 0.5* VDD	0.9	1	1.25	R_{ZQ}	1,2,3
		V_{OMdc}= 0.8* VDD	0.9	1	1.1	R_{ZQ}	1,2,3
		V_{OHdc}= 0.95* VDD	0.8	1	1.1	R_{ZQ}	1,2,3
MR32 for CK MR33 for CA & CS	80Ω	V_{OLdc}= 0.5* VDD	0.9	1	1.25	$R_{ZQ}/3$	1,2,3
		V_{OMdc}= 0.8* VDD	0.9	1	1.1	$R_{ZQ}/3$	1,2,3
		V_{OHdc}= 0.95* VDD	0.8	1	1.1	$R_{ZQ}/3$	1,2,3
MR32 for CK MR33 for CA & CS	60Ω	V_{OLdc}= 0.5* VDD	0.9	1	1.25	$R_{ZQ}/4$	1,2,3
		V_{OMdc}= 0.8* VDD	0.9	1	1.1	$R_{ZQ}/4$	1,2,3
		V_{OHdc}= 0.95* VDD	0.8	1	1.1	$R_{ZQ}/4$	1,2,3
MR32 for CK MR33 for CA & CS	40Ω	V_{OLdc}= 0.5* VDD	0.9	1	1.25	$R_{ZQ}/6$	1,2,3
		V_{OMdc}= 0.8* VDD	0.9	1	1.1	$R_{ZQ}/6$	1,2,3
		V_{OHdc}= 0.95* VDD	0.8	1	1.1	$R_{ZQ}/6$	1,2,3
Mismatch CA-CA within Device		0.8* VDD	tbd		tbd	%	1,2,4

NOTES:

1 - The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.

2 - Pull-up ODT resistors are recommended to be calibrated at 0.8*VDD. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5*VDD and 0.95*VDD.

3 - Measurement definition for RTT:tbd

4 - CA to CA mismatch within device variation for a given component including CS, CK_t and CK_c (characterized)

6 AC & DC Operating Conditions

6.1 Absolute Maximum Ratings - No Ballot

Table 90 — Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 2.5	V	4
V_{IN}, V_{OUT}	Voltage on any pin except VREFCA relative to Vss	-0.3 ~ 1.5	V	1,3,5
T_{STG}	Storage Temperature	-55 to +100	°C	1,2

NOTE
1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times;and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300 mV
4. VPP must be equal or greater than VDD/VDDQ at all times.
5.Overshoot area above 1.5 V is specified in Section 8.3.4, Section 8.3.5, and Section 8.3.6.

7 AC & DC Global Definitions

7.1 Transmitter (Tx), Receiver (Rx) and Channel Definitions - No Ballot

TBD

7.2 Bit Error Rate - Q2'17 Ballot #1849.12

7.2.1 Introduction

This section provides an overview of the Bit Error Rate (BER) and the desired Statistical Level of Confidence.

7.2.2 General Equation

$$n = \left(\frac{1}{BER}\right)\left[-\ln(1-SLC) + \ln\left(\sum_{k=0}^{N}\frac{(n\cdot BER)^k}{k!}\right)\right]$$

Where:

n = number of bits in a trial
SLC = statistical level of confidence
BER = Bit Error Rate
k = intermediate number of specific errors found in trial
N = number of errors recorded during trial

If no, errors are assumed in a given test period, the second term drops out and the equation becomes:

$$n = \left(\frac{1}{BER}\right)[-\ln(1-SLC)]$$

Intel recommends testing to 99.5% confidence levels; however, one may choose a number that is viable for their own manufacturing levels. To determine how many bits of data should be sent (again, assuming zero errors, or N=0), using BER=E^{-9} and confidence level SLC=99.5%, the result is n=(1/BER)(-ln(1-0.995) =5.298x10^9.

Results for commonly used confidence levels of 99.5% down to 70% are shown in **Table 7.2.3**.

Table 91 — Estimated Number of Transmitted Bits (n) for the confidence level of 70% to 99.5%

Number Errors	n = ln(1-SLC)/BER							
	99.5%	99%	95%	90%	85%	80%	75%	70%
0	5.298/BER	4.61/BER	2.99/BER	2.3/BER	1.90/BER	1.61/BER	1.39/BER	1.20/BER

7.2.3 Minimum Bit Error Rate (BER) Requirements

Table 92 specifies the UIavg and Bit Error Rate requirements over which certain receiver and transmitter timing and voltage specifications need to be validated assuming a 99.5% confidence level at BER=E^{-9}.

Table 92 — Minimum BER Requirements for Rx/Tx Timing and Voltage Tests for DDR5-3200 to 6400

Parameter	Symbol	DDR5-3200-4400			DDR5 4800-6400			Unit	Notes
		Min	Nom	Max	Min	Nom	Max		
Average UI	UI_{AVG}	0.999* nominal	1000/f	1.001* nominal	0.999* nominal	1000/f	1.001* nominal	ps	1
Number of UI (min)	$N_{Min\_UI\_Validation}$	$5.3x10^9$	-	-	$5.3x10^9$	-	-	UI	2
Bit Error Rate	BER_{Lane}	-	-	E^{-16}	-	-	E^{-16}	Events	3,4,5

NOTES:
1. Average UI size, “f” is data rate
2. # of UI over which certain Rx/Tx timing and voltage specifications need to be validated assuming a 99.5% confidence level at BER=E^{-9}.
3. This is a system parameter. It is the raw bit error rate for every lane before any logical PHY or link layer based correction. It may not be possible to have a validation methodology for this parameter for a standalone transmitter or standalone receiver, therefore, this parameter has to be validated in selected systems using a suitable methodology as deemed by the platform.
4. Bit Error Rate per lane. This is a raw bit error rate before any correction. This parameter is primarily used to determine electrical margins during electrical analysis and measurements that are located between two interconnected devices.
5. This is the minimum BER requirements for testing timing and voltage parameters listed in Input Clock Jitter, Rx DQS & DQ Voltage Sensitivity, Rx DQS Jitter Sensitivity, Rx DQ Stressed Eye, Tx DQS Jitter, Tx DQ Jitter, and Tx DQ Stressed EH/EW specifications.

7.3 Unit Interval and Jitter Definitions - Q2'17 Ballot #1849.11

This document describes the UI and NUI Jitter definitions associated with the Jitter parameters specified in Rx Stressed Eye, Tx DQS Jitter, Tx DQ Jitter and Input Clock Jitter specifications.

7.3.1 Unit Interval (UI)

The times at which the differential crossing points of the clock occur are defined at t1, t2, …, tn-1, tn,..., tK. The UI at index "n" is defined as shown in **Figure 80** (with n=1,2,…) from an arbitrary time in steady state, where n=0 is chosen as the starting crossing point.

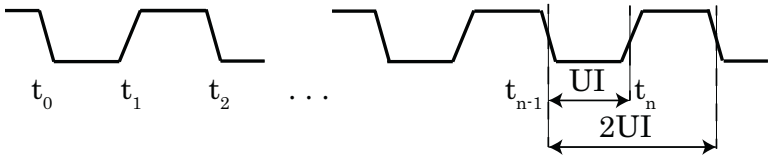
Mathematical definition of UI is shown in **Figure 80** and **Figure 81**.

Figure 80 — UI Definition in Terms of Adjacent Edge Timings

$$UI_n = t_n - t_{n-1}$$

For the Single-Ended data, the unit interval time starts when the signal crosses a pre-specified reference voltage. For the differential clock, the unit interval time starts when the CK_t and CK_c intersect (see **Figure 81**).

Figure 81 — UI Definition Using Clock Waveforms



7.3.2 UI Jitter Definition

If a number of UI edges are computed or measured at times t1, t2, …, tn-1, tn,..., tK, where K is the maximum number of samples, then the UI jitter at any instance "n" is defined in **Figure 82**, where T = the ideal UI size.

Figure 82 — UI Jitter for "nth" UI Definition (in terms of ideal UI)

$$UI(jit)_n = (t_n - t_{n-1}) - T \quad \text{where n=1,2,3,...,K}$$

In a large sample with random Gaussian-like jitter (therefore very close to symmetric distribution), the average of all UI sizes usually turns out to be very close to the ideal UI size.

The equation described in **Figure 82** assumes starting from an instant of steady state, where n=0 is chosen as the starting instant.

1 UI = one bit, which means 2 UI = one full cycle or time period of the forwarded strobe. Example: For 6.4 GT/s signaling, the forwarded strobe frequency is 3.2 GHz, or 1 UI = 156.25 ps.

Deterministic jitter is analyzed in terms of the peak-to-peak value and in terms of specific frequency components present in the jitter, isolating the causes for each frequency. Random jitter is unbounded and analyzed in terms of statistical distribution to convert to a bit error rate (BER) for the link.

7.3.3 UI-UI Jitter Definition

UI-UI (read as “UI to UI”) jitter is defined to be the jitter between two consecutive UI as shown in **Figure 83**.

Figure 83 — UI-UI Jitter Definitions

$$\Delta UI_n = UI_n - UI_{n-1} \quad \text{where n=2,3,...,K}$$

7.3.4 Accumulated Jitter (Over “N” UI)

Accumulated jitter is defined as the jitter accumulated over any consecutive “N” UI as shown in **Figure 84**.

Figure 84 — Definition of Accumulated Jitter (over “N” UI)

$$T_{acc}^{N} = \sum_{p=m}^{m+N-1}(UI_p - \overline{UI}) \quad \text{where m=1,2,...,K-N}$$

where UI is defined in the equation shown in **Figure 85**.

Figure 85 — Definition of $\overline{UI}$

$$\overline{UI} = \frac{\sum_{p=1}^{K} UI_p}{K} \quad \text{where p=1,2,...,N,...K}$$

8 AC & DC Input Measurement Levels

8.2 CA Rx voltage and timings - Q2'17 Ballot #1849.15

Note: The following draft assumes internal CA VREF. If the VREF is external, the specs will be modified accordingly.

The command and address (CA) including CS input receiver compliance mask for voltage and timing is shown in the figure below. All CA, CS signals apply the same compliance mask and operate in single data rate mode.

The CA input receiver mask for voltage and timing is shown in the figure below is applied across all CA pins. The receiver mask (Rx Mask) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal; it is not the valid data-eye.

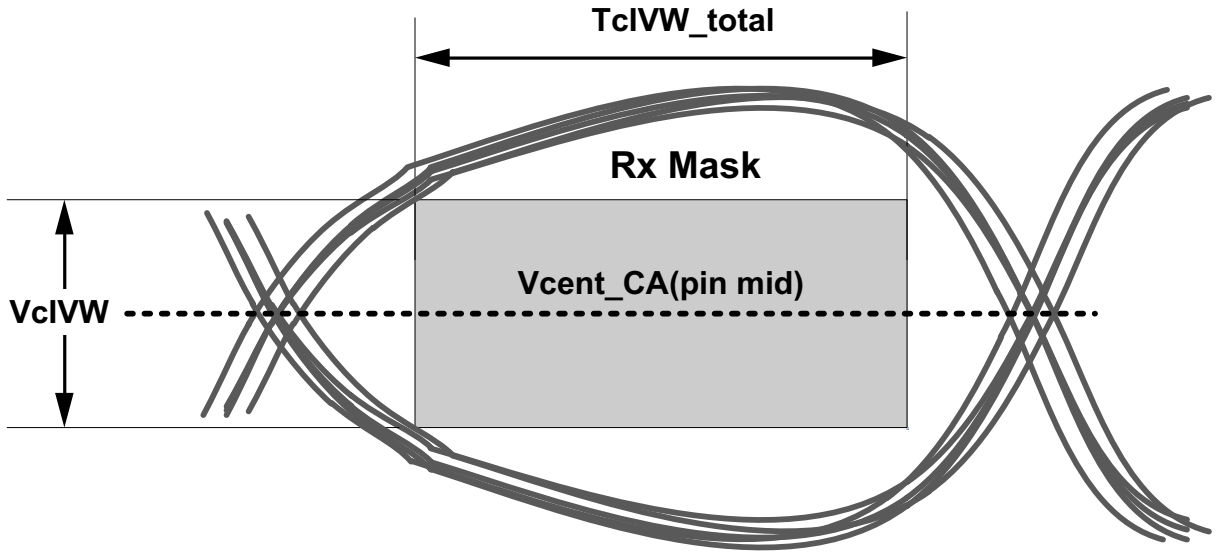


Figure 86 — CA Receiver (Rx) mask

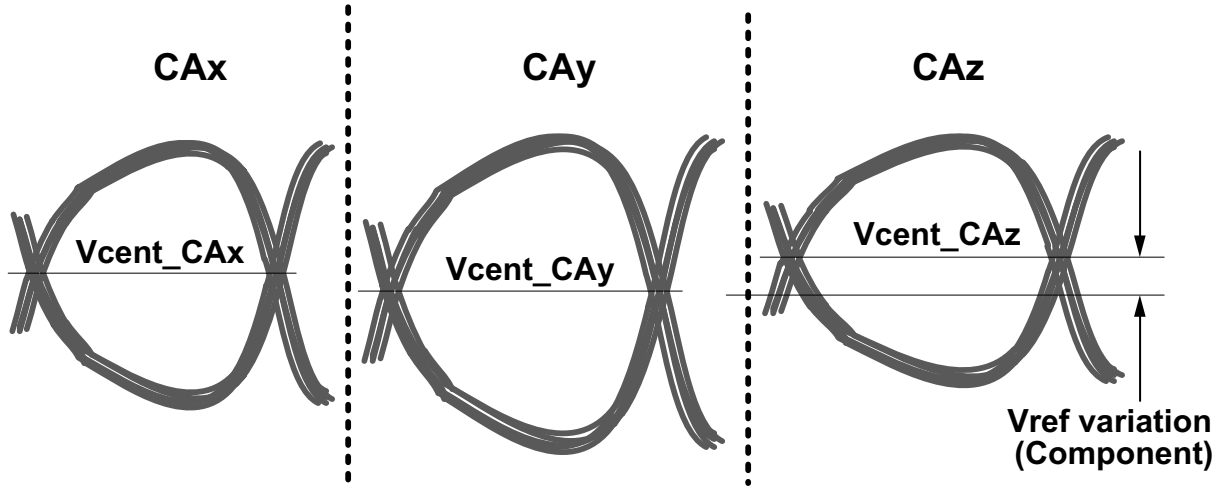
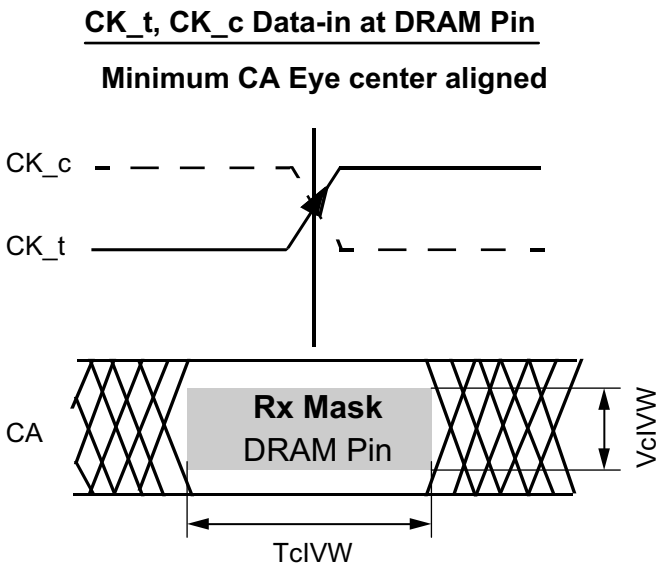


Figure 87 — Across pin V_{REF}CA voltage variation

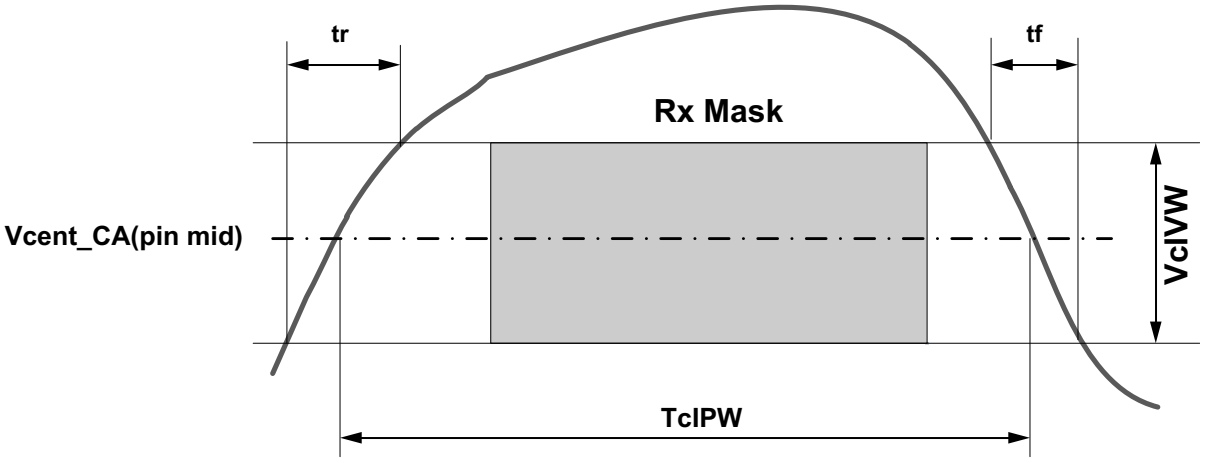
Vcent_CA(pin mid) is defined as the midpoint between the largest Vcent_CA voltage level and the smallest Vcent_CA voltage level across all CA and CS pins for a given DRAM component. Each CA Vcent level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in figure 149. This clarifies that any DRAM component level variation must be accounted for within the DRAM CA Rx mask. The component level V_{REF} will be set by the system to account for Ron and ODT settings.



TcIVW for all CA signals is defined as centered on the CK_t/CK_c crossing at the DRAM pin.

Figure 88 — CA Timings at the DRAM Pins

All of the timing terms in figure 3 are measured from the CK_t/CK_c to the center(midpoint) of the TcIVW window taken at the VcIVW_total voltage levels centered around Vcent_CA(pin mid).



Note
1. SRIN_cIVW=VcIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.

Figure 89 — CA TcIPW and SRIN_cIVW definition (for each input pulse)

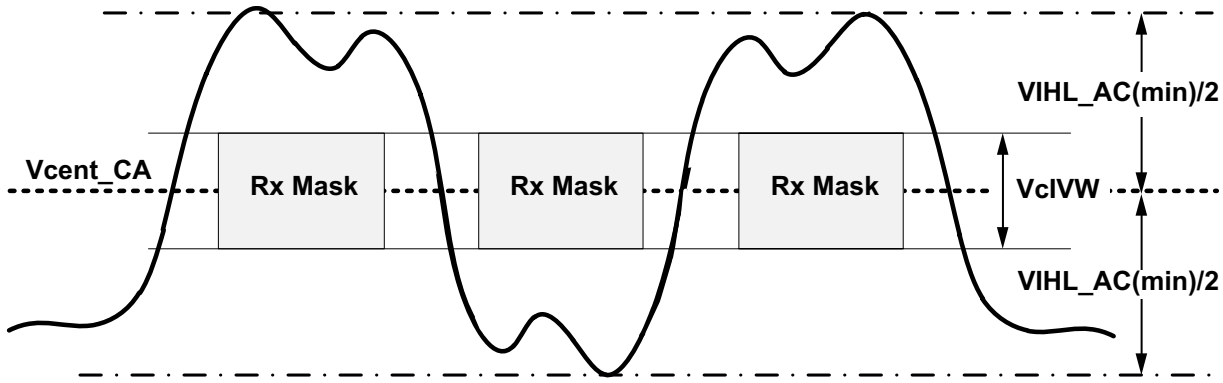


Figure 90 — CA VIHL_AC definition (for each input pulse)

Table 93 — DRAM CA, CS

*** UI=tck(avg)min**

Symbol	Parameter	DQ-3200[A]		DQ-4400		DQ-5200		DQ-6400		Unit	NOTE
		min	max	min	max	min	max	min	max		
VclVW	Rx Mask voltage - p-p	-	140	-	130	-	TBD	-	TBD	mV	1,2,4
TclVW	Rx timing window	-	0.2	-	0.20	-	TBD	-	TBD	UI*	1,2,3,4
VIHL_AC	CA input pulse amplitude	-	160	-	150	-	TBD	-	TBD	mV	7
TclPW	CA input pulse width	0.58		0.58		0.58		TBD		UI*	5
SRIN_clVW	Input Slew Rate over VclVW	1	7	1	7	1	7	1	7	V/ns	6
A. The following Rx voltage and absolute timing requirements apply for DQ operating frequencies at or below 3200 for all speed bins.											

Notes:

1. CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
2. Rx mask voltage VclVW total(max) must be centered around Vcent_CA(pin mid).
3. Rx differential CA to CK jitter total timing window at the VclVW voltage levels.
4. Defined over the CA internal V_{REF} range. The Rx mask at the pin must be within the internal V_{REF} CA range irrespective of the input signal common mode.
5. CA only minimum input pulse width defined at the Vcent_CA(pin mid).
6. Input slew rate over VclVW Mask centered at Vcent_CA(pin mid).
7. VIHL_AC does not have to be met when no transitions are occurring.

8.3 Clock Jitter - Q1'17 Ballot #1848.08

8.3.1 Overview

The clock is being driven to the DRAM either by the RCD for L/RDIMM modules, or by the host for U/SODIMM modules (**Figure 91**).

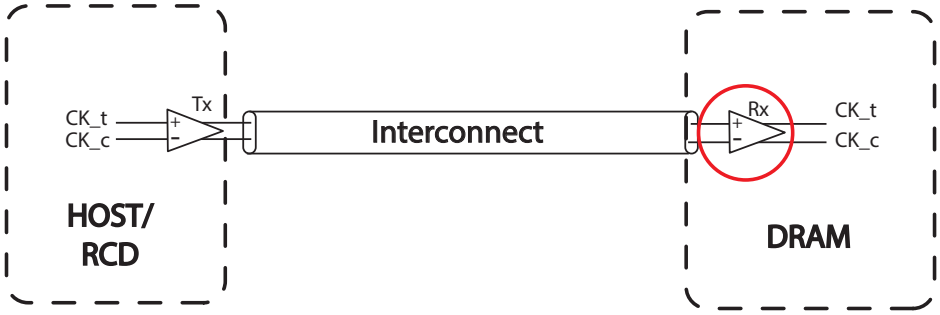


Figure 91 — RCD driving clock signals to the DRAM.

8.3.2 Specification for DRAM Input Clock Jitter

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. Input clock violating the min/max jitter values may result in malfunction of the DDR5 SDRAM device.

Table 94 — DRAM Input Clock Jitter Specifications for DDR5-3200 to 6400

[BUJ=Bounded Uncorrelated Jitter; DCD=Duty Cycle Distortion; Dj=Deterministic Jitter; Rj=Random Jitter; pp=Peak-to-Peak]

Parameter	Symbol	DDR5-3200		DDR5 3600		DDR5 4000		DDR5 4400-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
DRAM Reference clock frequency	fCK	0.9999* f0	1.0001* f0	0.9999* f0	1.0001* f0	0.9999* f0	1.0001* f0	0.9999* f0	1.0001* f0	MHz	1,11
Duty Cycle	tCK_Duty_UI	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	UI	11
Duty Cycle Error	tCK_Duty_UI_Error	-	0.0100	-	0.0075	-	0.0050	-	TBD	UI	1,4,11
Rj value of 1-UI Jitter	tCK_1UI_Rj_NoBUJ	-	0.0025	-	0.0025	-	0.0025	-	TBD	UI	3,5,11
Dj pp value of 1-UI Jitter	tCK_1UI_Dj_NoBUJ	-	0.0150	-	0.0125	-	0.0100	-	TBD	UI	3,6,11
Rj value of N-UI Jitter, where N=2,3	tCK_NUI_Rj_NoBUJ, where N=2,3	-	0.004	-	0.004	-	0.004	-	TBD	UI	3,7,11
Dj pp value of N-UI Jitter, where N=2,3	tCK_NUI_Dj_NoBUJ, where N=2,3	-	0.065	-	0.060	-	0.055	-	TBD	UI	3,8,11
Rj value of N-UI Jitter, where N=4,5,6,...,30	tCK_NUI_Rj_NoBUJ, where N=4,5,6,...,30	-	0.006	-	0.006	-	0.006	-	TBD	UI	3,9,11,12
Dj pp value of N-UI Jitter, N=4,5,6,...,30	tCK_NUI_Dj_NoBUJ, where N=4,5,6,...,30	-	0.085	-	0.080	-	0.075	-	TBD	UI	3,10,11,12

NOTE(S):
1.f0 = Data Rate/2, example: if data rate is 3200MT/s, then f0=1600
2. Rise and fall time slopes (V / nsec) are measured between +100 mV and -100 mV of the differential output of reference clock
3. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining Tx lanes send patterns to the corresponding Rx receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
4. Duty Cycle Error defined as absolute difference between average value of all UI with that of average of odd UI, which in magnitude would equal absolute difference between average of all UI and average of all even UI.
5. Rj value of 1-UI jitter without BUJ, but on-die system-like noise present. This extraction is to be done after software correction of DCD

6. Dj pp value of 1-UI jitter (after software assisted DCC). Without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
7. Rj value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. This extraction is to be done after software correction of DCD
8. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
9. Rj value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. This extraction is to be done after software correction of DCD
10. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
11. The validation methodology for these parameters will be covered in future ballots
12. If the clock meets total jitter Tj at BER of $1E^{-16}$, then meeting the individual Rj and Dj components of the spec can be considered optional. Tj is defined as Dj + 16.2*Rj for BER of $1E^{-16}$

8.4 Rx DQS Voltage Sensitivity - Q3'17 Ballot #1848.20

8.4.1 Overview

The receiver strobe input voltage sensitivity test provides the methodology for testing the receiver's sensitivity to varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise.

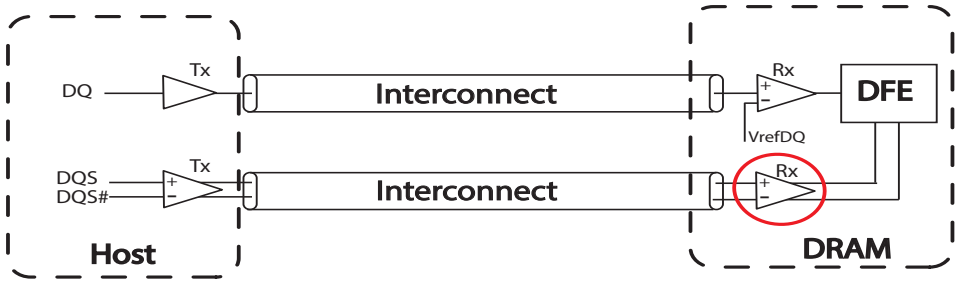


Figure 92 — Example of DDR5 Memory Interconnect

8.4.2 Receiver Strobe Voltage Sensitivity Parameter

Input differential (DQS_t, DQS_c) VRx_DQS is defined and measured as shown below. The receiver must pass the minimum BER requirements for DDR5.

Table 95 — Rx Strobe Input Voltage Sensitivity Parameter for DDR5-3200 to 6400

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Minimum DQS Rx input voltage sensitivity (differential pp)	VRx_DQS	-	85	-	75	-	70	-	TBD	mV	1,2

NOTE(S):
1. Refer to the minimum BER requirements for DDR5
2. The validation methodology for this parameter will be covered in future ballot(s)

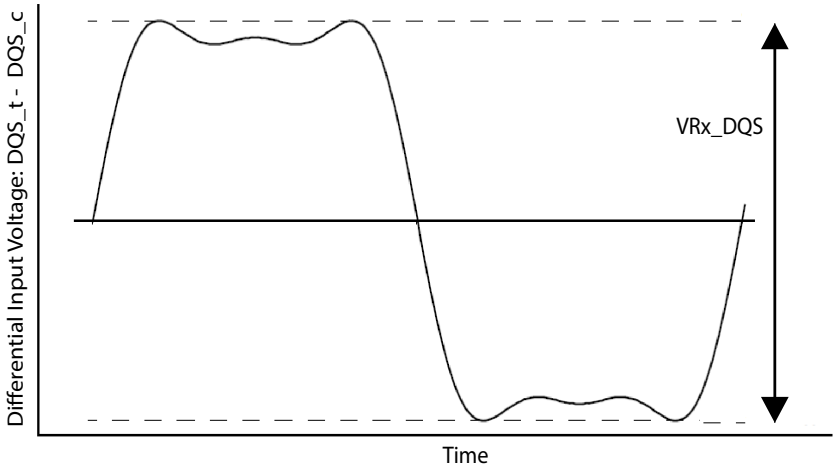


Figure 93 — VRx_DQS

8.5 Rx DQ Voltage Sensitivity - Q3'17 Ballot#1848.21

8.5.1 Overview

The receiver data input voltage sensitivity test provides the methodology for testing the receiver's sensitivity to varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter (Rj, Dj, DCD) and cross-talk noise.

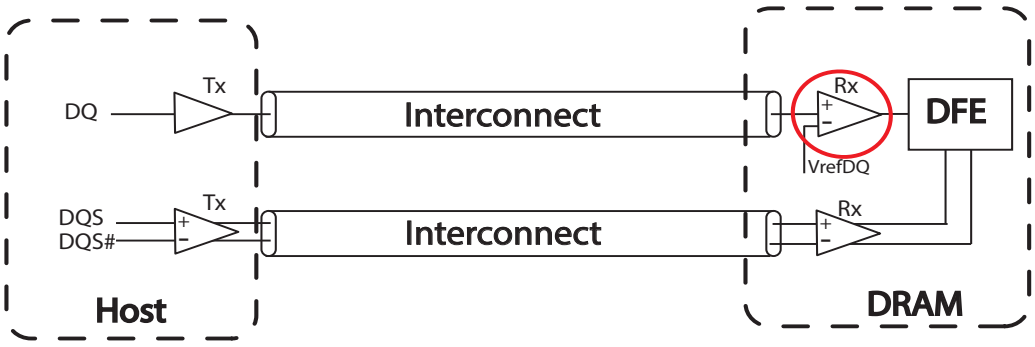


Figure 94 — Example of DDR5 Memory Interconnect

8.5.2 Receiver DQ Input Voltage Sensitivity Parameters

Input single-ended VRx_DQ is defined and measured as shown below. The receiver must pass the minimum BER requirements for DDR5.

Table 96 — Rx DQ Input Voltage Sensitivity Parameters for DDR5-3200 to 6400

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Minimum DQ Rx input voltage sensitivity applied around Vref	VRx_DQ	-	85	-	75	-	70	-	TBD	mV	1,2

NOTE(S):
1. Refer to the minimum BER requirements for DDR5
2. The validation methodology for this parameter will be covered in future ballot(s)

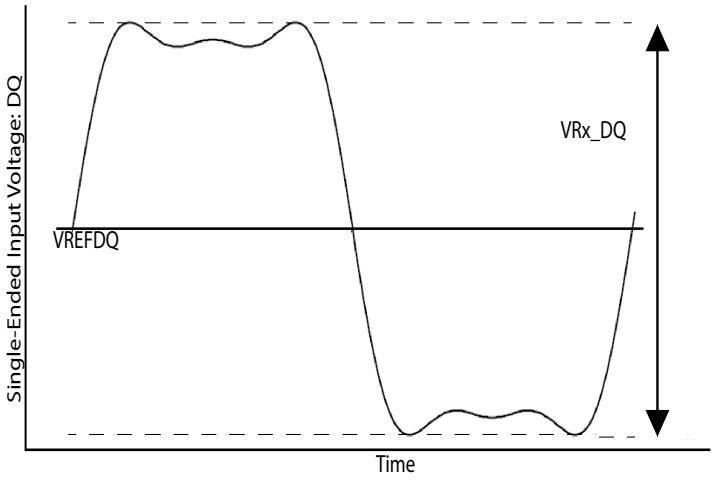


Figure 95 — VRx_DQ

9 AC & DC Output Measurement Levels and Timing

9.1 Output Driver DC Electrical Characteristics for DQS and DQ - Q1'17 Ballot #1848.04

The DDR5 driver supports two different Ron values. These Ron values are referred as strong(low Ron) and weak mode(high Ron). A functional representation of the output buffer is shown in the figure below.

Output driver impedance RON is defined as follows:

The individual pull-up and pull-down resistors (RON_{Pu} and RON_{Pd}) are defined as follows:

$$RON_{Pu} = \frac{VDDQ - Vout}{|I\ out|}$$ under the condition that RON_{Pd} is off

$$RON_{Pd} = \frac{Vout}{|I\ out|}$$ under the condition that RON_{Pu} is off

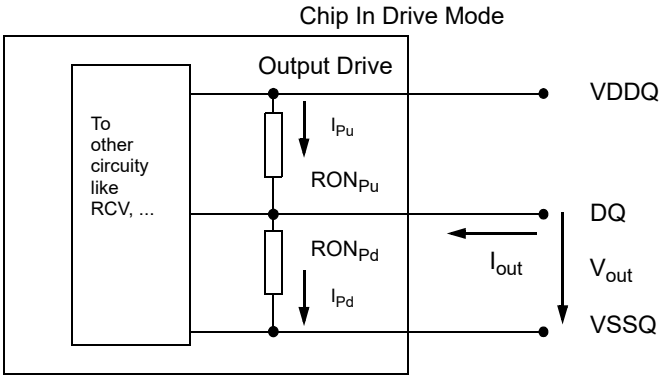


Table 97 — Output Driver DC Electrical Characteristics, assuming RZQ = 240ohm; entire operating temperature range; after proper ZQ calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	NOTE
34Ω	RON34Pd	VOLdc= 0.5*VDDQ	TBD	1	TBD	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	TBD	1	TBD	RZQ/7	1,2
		VOHdc= 0.95* VDDQ	TBD	1	TBD	RZQ/7	1,2
	RON34Pu	VOLdc= 0.5* VDDQ	TBD	1	TBD	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	TBD	1	TBD	RZQ/7	1,2
		VOHdc= 0.95* VDDQ	TBD	1	TBD	RZQ/7	1,2
48Ω	RON48Pd	VOLdc= 0.5*VDDQ	TBD	1	TBD	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	TBD	1	TBD	RZQ/5	1,2
		VOHdc= 0.95* VDDQ	TBD	1	TBD	RZQ/5	1,2
	RON48Pu	VOLdc= 0.5* VDDQ	TBD	1	TBD	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	TBD	1	TBD	RZQ/5	1,2
		VOHdc= 0.95* VDDQ	TBD	1	TBD	RZQ/5	1,2
Mismatch between pull-up and pull-down, MMPuPd		VOMdc= 0.8* VDDQ	-10		10	%	1,2,4,3
Mismatch DQ-DQ within byte variation pull-up, MMPudd		VOMdc= 0.8* VDDQ			10	%	1,2,4
Mismatch DQ-DQ within byte variation pull-dn, MMPddd		VOMdc= 0.8* VDDQ			10	%	1,2,4

NOTE :

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity(TBD).
2. Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8 * VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * VDDQ and 0.95 * VDDQ.
3. Measurement definition for mismatch between pull-up and pull-down, MMPuPd : Measure RONPu and RONPD both at 0.8*VDD separately;Ron-nom is the nominal Ron value

$$MMPuPd = \frac{RONPu - RONPd}{RONNOM} * 100$$

4. RON variance range ratio to RON Nominal value in a given component, including DQS_t and DQS_c.

$$MMPudd = \frac{RONPuMax - RONPuMin}{RONNOM} * 100$$

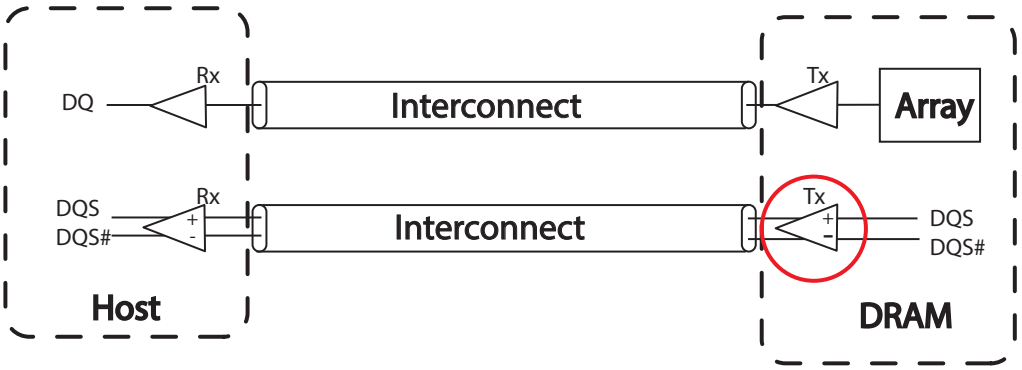
$$MMPddd = \frac{RONPdMax - RONPdMin}{RONNOM} * 100$$

5. This parameter of x16 device is specified for Upper byte and Lower byte.

9.2 Tx DQS Jitter - Q1'17 Ballot #1848.09

9.2.1 Overview

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. The DDR5 device output jitter must not exceed maximum values specified in **Table 98**.



9.2.2 DQS Tx Jitter Parameters

Table 98 — Tx DQS Jitter Parameters for DDR5-3200 to 6400

[Dj=Deterministic Jitter; Rj=Random Jitter; DCD=Duty Cycle Distortion; BUJ=Bounded Uncorrelated Jitter; pp=Peak to Peak]

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Strobe Duty Cycle Error	tTx_DQS_Duty_UI	-	0.0150	-	0.0125	-	0.0100	-	TBD	UI	3,4
Rj Value of 1-UI Jitter without BUJ	tTx_DQS_1UI_Rj_NoBUJ	-	0.00375	-	0.00375	-	0.00375	-	TBD	UI	1,3,5
Dj pp Value of 1-UI Jitter without BUJ	tTx_DQS_1UI_Dj_NoBUJ	-	0.025	-	0.0175	-	0.015	-	TBD	UI	3,6
Rj Value of N-UI jitter without BUJ, where 1<N< 4	tTx_DQS_NUI_Rj_NoBUJ	-	0.006	-	0.006	-	0.006	-	TBD	UI	3,7
Dj pp Value of N-UI Jitter without BUJ, where 1<N < 4	tTx_DQS_NUI_Dj_NoBUJ	-	0.085	-	0.08	-	0.075	-	TBD	UI	3,8

NOTE(S):

1. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases,the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
2. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases the contribution of BUJ is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers, so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
3. The validation methodology for these parameters will be covered in future ballots
4. Strobe duty cycle error, defined as absolute difference between average value of all UI with that of average of odd UI, which in magnitude would equal absolute difference between average of all UI and average of all even UI.
5. Rj value of 1-UI jitter. Without BUJ, but on-die system like noise present. This extraction is to be done after software correction of DCD
6. Dj pp value of 1-UI jitter (after software assisted DCC). Without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
7. Rj Value of N-UI jitter, Without BUJ but on-die system like noise present, where < N < 4. This extraction is to be done after software correction of DCD
8. Dj pp value of N-UI jitter. Without BUJ, but on-die system like noise present, where 1 < N < 4. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD

9.2.3 Minimum BER Requirements for Rx/Tx Voltage and Timing Tests

Table 99 specifies the UIavg and Bit Error Rate requirements over which certain receiver/ transmitter timing and voltage specifications need to be validated assuming a 99.5% confidence level at 10^{-9} BER.

Table 99 — Minimum BER Requirements for Rx/Tx Timing and Voltage Tests for DDR5-3200 to 6400

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5 4000		DDR5 4400-6400		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Average UI	UI_{AVG}	0.999* nominal	1.001* nominal	0.999* nominal	1.001* nominal	0.999* nominal	1.001* nominal	0.999* nominal	1.001* nominal	ps	2,3,6
Number of UI (min)	$N_{Min\_UI\_Validation}$	$5.3x10^9$	-	$5.3x10^9$	-	$5.3x10^9$	-	TBD	-	UI	2,4,6
Bit Error Rate	BER_{Lane}	-	10^{-16}	-	10^{-16}	-	10^{-16}	-	TBD	Events	1,2,4, 5,6

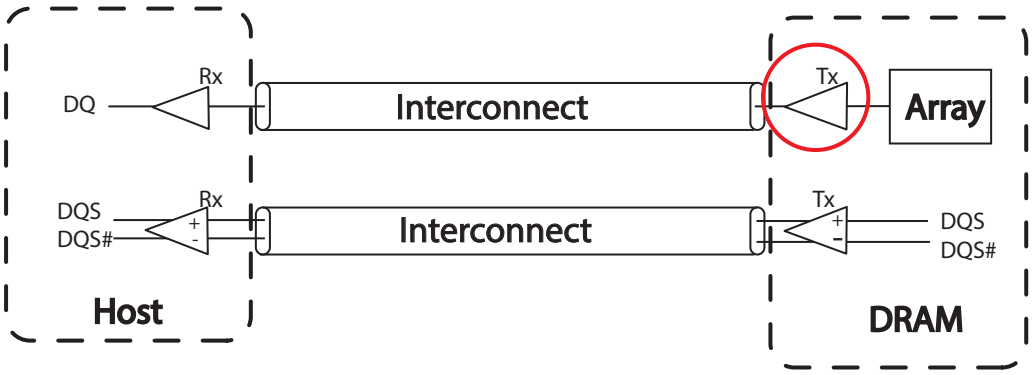
NOTE(S):

1. This is a system parameter. It is the raw bit error rate for every lane before any logical PHY or link layer based correction. It is not possible to have a validation methodology for this parameter for a standalone transmitter or standalone receiver, therefore this parameter has to be validated in selected systems using a suitable methodology as deemed by the platform
2. The validation methodologies for these specs are dependent almost solely on the validation hooks built into the silicon itself and thus are determined by the designer and cannot be called out here
3. Average UI size “f” is data rate
4. # of UI over which the eye mask voltage and timing spec needs to be validated assuming a 99.5% confidence level at 10-9 BER
5. Bit Error Rate per lane. This is a raw bit error rate before any correction. This parameter is primarily used to determine electrical margins during electrical analysis and measurements that are located between two interconnected devices.
6. This is the minimum BER requirements for testing timing and voltage parameters listed in Clock Jitter, Rx DQS & DQ Voltage Sensitivity, Rx DQS Jitter Sensitivity, Rx Stressed Eye, Tx DQS Jitter, Tx DQ Jitter, and Tx Stressed Eye specifications

9.3 Tx DQ Jitter - Q1'17 Ballot #1848.10

9.3.1 Overview

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. The DDR5 device output jitter must not exceed maximum values specified in **Table 100**.



9.3.2 Tx DQ Jitter Parameters

Table 100 — Tx DQ Jitter Parameters for DDR5-3200 to 6400

[Dj=Deterministic Jitter; Rj=Random Jitter; DCD=Duty Cycle Distortion; BUJ=Bounded Uncorrelated Jitter; pp=Peak to Peak]

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
DQ Duty Cycle Error	tTx_DQ_Duty_UI	-	0.0150	-	0.0125	-	0.0100	-	TBD	UI	3,4,10
Rj of 1-UI jitter without BUJ	tTx_DQ_1UI_Rj_NoBUJ	-	0.00375	-	0.00375	-	0.00375	-	TBD	UI	1,3,5, 9
Dj pp 1-UI jitter without BUJ	tTx_DQ_1UI_Dj_NoBUJ	-	0.0250	-	0.0175	-	0.0150	-	TBD	UI	3,6,9
Rj of N-UI jitter without BUJ, where 1<N<4	tTx_DQ_NUI_Rj_NoBUJ	-	0.006	-	0.006	-	0.006	-	TBD	UI	3,7,9
Dj pp N-UI jitter without BUJ, where 1<N<4	tTx_DQ_NUI_Dj_NoBUJ	-	0.085	-	0.080	-	0.075	-	TBD	UI	3,8, 10
Delay of any data lane relative to strobe lane	tTx_DQS2DQ_Skew	-0.25	0.25	-0.25	0.25	-0.25	0.25	TBD	TBD	UI	3,9,10

NOTES:

1. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.
2. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of BUJ is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
3. The validation methodology for these parameters will be covered in future ballots
4. DQ Duty Cycle Error, defined as absolute difference between average value of all UI with that of average of odd UI, which in magnitude would equal absolute difference between average of all UI and average of all even UI.
5. Rj value of 1-UI jitter without BUJ, but on-die system like noise present. This extraction is to be done after software correction of DCD

6. Dj pp value of 1-UI jitter (after software assisted DCC). Without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
7. Rj value of N-UI jitter without BUJ, but on-die system like noise present, where 1 < N < 4. This extraction is to be done after software correction of DCD
8. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present, where 1 < N < 4. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
9. Delay of any data lane relative to strobe lane, as measured at Tx output
10. Vref noise level to DQ jitter should be adjusted to minimize DCD

9.3.3 Minimum BER Requirements for Rx/Tx Voltage and Timing Tests

Table 2 specifies the UIavg and Bit Error Rate requirements over which certain receiver/ transmitter timing and voltage specifications need to be validated assuming a 99.5% confidence level at 10^{-9} BER.

Table 101 — Minimum BER Requirements for Rx/Tx Timing and Voltage Tests for DDR5-3200 to 6400

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400-6400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Average UI	UI_{AVG}	0.999* nominal	1.001* nominal	0.999* nominal	1.001* nominal	0.999* nominal	1.001* nominal	0.999* nominal	1.001* nominal	ps	2,3,6
Number of UI (min)	$N_{Min\_UI\_Validation}$	$5.3x10^9$	-	$5.3x10^9$	-	$5.3x10^9$	-	TBD	-	UI	2,4,6
Bit Error Rate	BER_{Lane}	-	10^{-16}	-	10^{-16}	-	10^{-16}	-	TBD	Events	1,2,4,5,6

NOTES:
1. This is a system parameter. It is the raw bit error rate for every lane before any logical PHY or link layer based correction. It is not possible to have a validation methodology for this parameter for a standalone transmitter or standalone receiver, therefore this parameter has to be validated in selected systems using a suitable methodology as deemed by the platform.
2. The validation methodologies for these specs are dependent almost solely on the validation hooks built into the silicon itself and, thus, are determined by the designer and cannot be called out here.
3. Average UI size, “f” is data rate
4. # of UI over which the eye mask voltage and timing spec needs to be validated assuming a 99.5% confidence level at 10-9 BER
5. Bit Error Rate per lane. This is a raw bit error rate before any correction. This parameter is primarily used to determine electrical margins during electrical analysis and measurements that are located between two interconnected devices.
6. This is the minimum BER requirements for testing timing and voltage parameters listed in Clock Jitter, Rx DQS & DQ Voltage Sensitivity, Rx DQS Jitter Sensitivity, Rx Stressed Test, Tx DQS Jitter, Tx DQ Jitter, and Tx Stressed Eye specifications

10 Speed Bins

DDR5 Standard Speed Bins defined as:
3200 / 3600 / 4000 / 4400 / 4800 / 5200 / 5600 / 6000 / 6400

Future Speed Bins, (which are just placeholders) are defined as:
6800 / 7200 / 7600 / 8000 / 8400

10.1 DDR5-3200 Speed Bins and Operations - Q3'16 Ballot #1830.35A

Table 102 — DDR5-3200 Speed Bins and Operations

Speed Bin		DDR5-3200A		DDR5-3200B		DDR5-3200C		Unit	NOTE
CL-nRCD-nRP		25-25-25		26-26-26		28-28-28			
Parameter	Symbol	min	max	min	max	min	Max		
Internal read command to first data	tAA	15.63		16.25		17.50		ns	
ACT to internal read or write delay time	tRCD	15.63		16.25		17.50		ns	
Row Precharge Time	tRP	15.63		16.25		17.50		ns	
ACT to PRE command period	tRAS	32.00	9 x tREFI	32.00	9 x tREFI	32.00	9 x tREFI	ns	
ACT to ACT or REF command period	tRC	47.63		48.25		49.50		ns	
CAS Write Latency,	CWL	CWL=CL (25)		CWL=CL (27)		CWL=CL (28)		ns	
CWL=CL=25	tCK(AVG)							ns	
CWL=CL=27	tCK(AVG)							ns	
CWL=CL=28	tCK(AVG)							ns	
Supported CL, CWL Settings		25		26		28		nCK	

10.2 DDR5-3600 Speed Bins and Operations - Q3'16 Ballot #1830.35A

Table 103 — DDR5-3600 Speed Bins and Operations

Speed Bin		DDR5-3600A		DDR5-3600B		DDR5-3600C		Unit	NOTE
CL-nRCD-nRP		28-28-28		30-30-30		33-33-33			
Parameter	**Symbol**	min	max	min	max	min	Max		
Internal read command to first data	tAA	15.56		16.67		18.33		ns	
ACT to internal read or write delay time	tRCD	15.56		16.67		18.33		ns	
Row Precharge Time	tRP	15.56		16.67		18.33		ns	
ACT to PRE command period	tRAS	32.00	9 x tREFI	32.00	9 x tREFI	32.00	9 x tREFI	ns	
ACT to ACT or REF command period	tRC	47.56		48.67		50.33		ns	
CAS Write Latency,	CWL	CWL=CL (28)		CWL=CL (30)		CWL=CL (33)		ns	
CWL=CL=25	tCK(AVG)							ns	
CWL=CL=27	tCK(AVG)							ns	
CWL=CL=28	tCK(AVG)							ns	
Supported CL, CWL Settings		28		30		33		nCK	

10.3 DDR5-4000 Speed Bins and Operations - Q3'16 Ballot #1830.35A

Table 104 — DDR5-4000 Speed Bins and Operations

Speed Bin		DDR5-4000A		DDR5-4000B		DDR5-4000C		Unit	NOTE
CL-nRCD-nRP		30-30-30		33-33-33		36-36-36			
Parameter	Symbol	min	max	min	max	min	Max		
Internal read command to first data	tAA	15.00		16.50		18.00		ns	
ACT to internal read or write delay time	tRCD	15.00		16.50		18.00		ns	
Row Precharge Time	tRP	15.00		16.50		18.00		ns	
ACT to PRE command period	tRAS	32.00	9 x tREFI	32.00	9 x tREFI	32.00	9 x tREFI	ns	
ACT to ACT or REF command period	tRC	47.00		48.50		50.00		ns	
CAS Write Latency,	CWL	CWL=CL (30)		CWL=CL (33)		CWL=CL (36)		ns	
CWL=CL=25	tCK(AVG)							ns	
CWL=CL=27	tCK(AVG)							ns	
CWL=CL=28	tCK(AVG)							ns	
Supported CL, CWL Settings		30		33		36		nCK	

10.4 DDR5-4400 Speed Bins and Operations - Q3'16 Ballot #1830.35A

Table 105 — DDR5-4400 Speed Bins and Operations

Speed Bin		DDR5-4400A		DDR5-4400B		DDR5-4400C		Unit	NOTE
CL-nRCD-nRP		33-33-33		36-36-36		39-39-39			
Parameter	Symbol	min	max	min	max	min	Max		
Internal read command to first data	tAA	15.00		16.36		17.73		ns	
ACT to internal read or write delay time	tRCD	15.00		16.36		17.73		ns	
Row Precharge Time	tRP	15.00		16.36		17.73		ns	
ACT to PRE command period	tRAS	32.00	9 x tREFI	32.00	9 x tREFI	32.00	9 x tREFI	ns	
ACT to ACT or REF command period	tRC	47.00		48.36		49.73		ns	
CAS Write Latency,	CWL	CWL=CL (33)		CWL=CL (36)		CWL=CL (39)		ns	
CWL=CL=25	tCK(AVG)							ns	
CWL=CL=27	tCK(AVG)							ns	
CWL=CL=28	tCK(AVG)							ns	
Supported CL, CWL Settings		33		36		39		nCK	

10.5 DDR5-5200 Speed Bins and Operations - No Ballot

Table 106 — DDR5-5200 Speed Bins and Operations

Speed Bin		DDR5-5200A		DDR5-5200B		DDR5-5200C		Unit	NOTE
CL-nRCD-nRP									
Parameter	Symbol	min	max	min	max	min	Max		
Internal read command to first data	tAA	15.00		16.50		18.00		ns	
ACT to internal read or write delay time	tRCD	15.00		16.50		18.00		ns	
Row Precharge Time	tRP	15.00		16.50		18.00		ns	
ACT to PRE command period	tRAS		9 x tREFI		9 x tREFI		9 x tREFI	ns	
ACT to ACT or REF command period	tRC	47.00						ns	
CAS Write Latency,	CWL	CWL=CL-2		CWL=CL-2		CWL=CL-2		ns	
CWL=CL=TBD	tCK(AVG)							ns	
CWL=CL=TBD	tCK(AVG)							ns	
CWL=CL=TBD	tCK(AVG)							ns	
Supported CL, CWL Settings								nCK	

10.6 DDR5-5600 Speed Bins and Operations - No Ballot

Table 107 — DDR5-5600 Speed Bins and Operations

Speed Bin		DDR5-5600A		DDR5-5600B		DDR5-5600C		Unit	NOTE
CL-nRCD-nRP									
Parameter	Symbol	min	max	min	max	min	Max		
Internal read command to first data	tAA	15.00		16.50		18.00		ns	
ACT to internal read or write delay time	tRCD	15.00		16.50		18.00		ns	
Row Precharge Time	tRP	15.00		16.50		18.00		ns	
ACT to PRE command period	tRAS		9 x tREFI		9 x tREFI		9 x tREFI	ns	
ACT to ACT or REF command period	tRC	47.00						ns	
CAS Write Latency,	CWL	CWL=CL-2		CWL=CL-2		CWL=CL-2		ns	
CWL=CL=TBD	tCK(AVG)							ns	
CWL=CL=TBD	tCK(AVG)							ns	
CWL=CL=TBD	tCK(AVG)							ns	
Supported CL, CWL Settings								nCK	

10.7 DDR5-6000 Speed Bins and Operations - No Ballot

Table 108 — DDR5-6000 Speed Bins and Operations

Speed Bin		DDR5-6000A		DDR5-6000B		DDR5-6000C		Unit	NOTE
CL-nRCD-nRP									
Parameter	Symbol	min	max	min	max	min	Max		
Internal read command to first data	tAA	15.00		16.50		18.00		ns	
ACT to internal read or write delay time	tRCD	15.00		16.50		18.00		ns	
Row Precharge Time	tRP	15.00		16.50		18.00		ns	
ACT to PRE command period	tRAS		9 x tREFI		9 x tREFI		9 x tREFI	ns	
ACT to ACT or REF command period	tRC	47.00						ns	
CAS Write Latency,	CWL	CWL=CL-2		CWL=CL-2		CWL=CL-2		ns	
CWL=CL=TBD	tCK(AVG)							ns	
CWL=CL=TBD	tCK(AVG)							ns	
CWL=CL=TBD	tCK(AVG)							ns	
Supported CL, CWL Settings								nCK	

10.8 DDR5-6400 Speed Bins and Operations - No Ballot

Table 109 — DDR5-6400 Speed Bins and Operations

Speed Bin		DDR5-6400A		DDR5-6400B		DDR5-6400C		Unit	NOTE
CL-nRCD-nRP									
Parameter	Symbol	min	max	min	max	min	Max		
Internal read command to first data	tAA	15.00		16.50		18.00		ns	
ACT to internal read or write delay time	tRCD	15.00		16.50		18.00		ns	
Row Precharge Time	tRP	15.00		16.50		18.00		ns	
ACT to PRE command period	tRAS		9 x tREFI		9 x tREFI		9 x tREFI	ns	
ACT to ACT or REF command period	tRC	47.00						ns	
CAS Write Latency,	CWL	CWL=CL-2		CWL=CL-2		CWL=CL-2		ns	
CWL=CL=TBD	tCK(AVG)							ns	
CWL=CL=TBD	tCK(AVG)							ns	
CWL=CL=TBD	tCK(AVG)							ns	
Supported CL, CWL Settings								nCK	

10.9 DDR5-6800 Speed Bins and Operations - (Future Bin Placeholder) No Ballot

Table 110 — DDR5-6800 Speed Bins and Operations

Speed Bin		DDR5-6800A		DDR5-6800B		DDR5-6800C		Unit	NOTE
CL-nRCD-nRP									
Parameter	Symbol	min	max	min	max	min	Max		
Internal read command to first data	tAA	15.00		16.50		18.00		ns	
ACT to internal read or write delay time	tRCD	15.00		16.50		18.00		ns	
Row Precharge Time	tRP	15.00		16.50		18.00		ns	
ACT to PRE command period	tRAS		9 x tREFI		9 x tREFI		9 x tREFI	ns	
ACT to ACT or REF command period	tRC	47.00						ns	
CAS Write Latency,	CWL	CWL=CL-2		CWL=CL-2		CWL=CL-2		ns	
CWL=CL=TBD	tCK(AVG)							ns	
CWL=CL=TBD	tCK(AVG)							ns	
CWL=CL=TBD	tCK(AVG)							ns	
Supported CL, CWL Settings								nCK	

10.10 DDR5-7200 Speed Bins and Operations - (Future Bin Placeholder) No Ballot

Table 111 — DDR5-7200 Speed Bins and Operations

Speed Bin		DDR5-7200A		DDR5-7200B		DDR5-7200C		Unit	NOTE
CL-nRCD-nRP									
Parameter	Symbol	min	max	min	max	min	Max		
Internal read command to first data	tAA	15.00		16.50		18.00		ns	
ACT to internal read or write delay time	tRCD	15.00		16.50		18.00		ns	
Row Precharge Time	tRP	15.00		16.50		18.00		ns	
ACT to PRE command period	tRAS		9 x tREFI		9 x tREFI		9 x tREFI	ns	
ACT to ACT or REF command period	tRC	47.00						ns	
CAS Write Latency,	CWL	CWL=CL-2		CWL=CL-2		CWL=CL-2		ns	
CWL=CL=TBD	tCK(AVG)							ns	
CWL=CL=TBD	tCK(AVG)							ns	
CWL=CL=TBD	tCK(AVG)							ns	
Supported CL, CWL Settings								nCK	

10.11 DDR5-7600 Speed Bins and Operations - (Future Bin Placeholder) No Ballot

Table 112 — DDR5-7600 Speed Bins and Operations

Speed Bin		DDR5-7600A		DDR5-7600B		DDR5-7600C		Unit	NOTE
CL-nRCD-nRP									
Parameter	Symbol	min	max	min	max	min	Max		
Internal read command to first data	tAA	15.00		16.50		18.00		ns	
ACT to internal read or write delay time	tRCD	15.00		16.50		18.00		ns	
Row Precharge Time	tRP	15.00		16.50		18.00		ns	
ACT to PRE command period	tRAS		9 x tREFI		9 x tREFI		9 x tREFI	ns	
ACT to ACT or REF command period	tRC	47.00						ns	
CAS Write Latency,	CWL	CWL=CL-2		CWL=CL-2		CWL=CL-2		ns	
CWL=CL=TBD	tCK(AVG)							ns	
CWL=CL=TBD	tCK(AVG)							ns	
CWL=CL=TBD	tCK(AVG)							ns	
Supported CL, CWL Settings								nCK	

10.12 DDR5-8000 Speed Bins and Operations - (Future Bin Placeholder) No Ballot

Table 113 — DDR5-8000 Speed Bins and Operations

Speed Bin		DDR5-8000A		DDR5-8000B		DDR5-8000C		Unit	NOTE
CL-nRCD-nRP									
Parameter	Symbol	min	max	min	max	min	Max		
Internal read command to first data	tAA	15.00		16.50		18.00		ns	
ACT to internal read or write delay time	tRCD	15.00		16.50		18.00		ns	
Row Precharge Time	tRP	15.00		16.50		18.00		ns	
ACT to PRE command period	tRAS		9 x tREFI		9 x tREFI		9 x tREFI	ns	
ACT to ACT or REF command period	tRC	47.00						ns	
CAS Write Latency,	CWL	CWL=CL-2		CWL=CL-2		CWL=CL-2		ns	
CWL=CL=TBD	tCK(AVG)							ns	
CWL=CL=TBD	tCK(AVG)							ns	
CWL=CL=TBD	tCK(AVG)							ns	
Supported CL, CWL Settings								nCK	

10.13 DDR5-8400 Speed Bins and Operations - (Future Bin Placeholder) No Ballot

Table 114 — DDR5-8400 Speed Bins and Operations

Speed Bin		DDR5-8400A		DDR5-8400B		DDR5-8400C		Unit	NOTE
CL-nRCD-nRP									
Parameter	Symbol	min	max	min	max	min	Max		
Internal read command to first data	tAA	15.00		16.50		18.00		ns	
ACT to internal read or write delay time	tRCD	15.00		16.50		18.00		ns	
Row Precharge Time	tRP	15.00		16.50		18.00		ns	
ACT to PRE command period	tRAS		9 x tREFI		9 x tREFI		9 x tREFI	ns	
ACT to ACT or REF command period	tRC	47.00						ns	
CAS Write Latency,	CWL	CWL=CL-2		CWL=CL-2		CWL=CL-2		ns	
CWL=CL=TBD	tCK(AVG)							ns	
CWL=CL=TBD	tCK(AVG)							ns	
CWL=CL=TBD	tCK(AVG)							ns	
Supported CL, CWL Settings								nCK	

11 IDD and IDDQ Specification Parameters and Test conditions - No Ballot

11.1 IDD, IPP and IDDQ Measurement Conditions - No Ballot

In this chapter, IDD, IPP and IDDQ measurement conditions such as test load and patterns are defined. Figure 203 shows the setup and test load for IDD, IPP and IDDQ measurements.

TBD

TBD

Figure 96 — Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements

TBD

Figure 97 — Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement.

Table 115 — Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns

11.2 IDD Specifications

IDD and IPP values are for full operating range of voltage and temperature unless otherwise noted. IDD and IPP values are for full operating range of voltage and temperature unless otherwise noted.

Table 126 — I_{DD} and I_{DDQ} Specification Example

Speed Grade Bin				
Symbol	**IDD Max.**	**IPP Max.**	**Unit**	**NOTE**
I_{DD0}			mA	
I_{DD0A}			mA	
I_{DD1}			mA	
I_{DD1A}			mA	
I_{DD2N}			mA	
I_{DD2NA}			mA	
I_{DD2NT}			mA	
I_{DDQ2NT}			mA	
I_{DD2NL}			mA	
I_{DD2NG}			mA	
I_{DD2ND}			mA	
I_{DD2N_par}			mA	
I_{DD2P}			mA	
I_{DD2Q}			mA	
I_{DD3N}			mA	
I_{DD3NA}			mA	
I_{DD3P}			mA	
I_{DD4R}			mA	
I_{DD4RA}			mA	
I_{DD4RB}			mA	
I_{DDQ4R}			mA	
I_{DDQ4RB}			mA	
I_{DD4W}			mA	
I_{DD4WA}			mA	
I_{DD4WB}			mA	
I_{DD4WC}			mA	
I_{DD4W_par}			mA	
I_{DD5B}			mA	
I_{DD5F2}			mA	
I_{DD5F4}			mA	
I_{DD6N}			mA	
I_{DD6E}			mA	
I_{DD6N}			mA	
I_{DD6E}[1]			mA	
I_{DD6R}			mA	
I_{DD6A}			mA	
I_{DD7}			mA	
I_{DD8}			mA	

NOTE 1 Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR5 SDRAM devices support the following options or requirements referred to in this material.

Table 127 — I_{PP} Specification Example

Speed Grade Bin			Unit	NOTE
Symbol	IDD Max.	IPP Max.		
I_{PP0}			mA	
I_{PP1}			mA	
I_{PP2N}			mA	
I_{PP2P}			mA	
I_{PP3N}			mA	
I_{PP3P}			mA	
I_{PP4R}			mA	
I_{PP4W}			mA	
I_{PP5B}			mA	
I_{PP5F2}			mA	
I_{PP5F4}			mA	
I_{PP5TC}			mA	
I_{PP6N}			mA	
I_{PP6E}			mA	
I_{PP6N}			mA	
I_{PP6E}[1]			mA	
I_{PP6R}			mA	
I_{PP6A}			mA	
I_{PP7}			mA	
I_{PP8}			mA	

NOTE 1 Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR5 SDRAM devices support the following options or requirements referred to in this material.

Table 128 — I_{DD6} Specification

Symbol	Temperature Range	Value	Unit	NOTE
I_{DD6N}	0 - 85 °C		mA	3,4
I_{DD6E}	0 - 95 °C		mA	4,5,6
I_{DD6R}	0 - 45°C		mA	4,6,9
I_{DD6A}	0 °C ~ T_a		mA	4,6,7,8
	T_b ~ T_y		mA	4,6,7,8
	T_z ~ $T_{OPERmax}$		mA	4,6,7,8

NOTE 1 Some I_{DD} currents are higher for x16 organization due to larger page-size architecture.
NOTE 2 Max. values for I_{DD} currents considering worst case conditions of process, temperature and voltage.
NOTE 3 Applicable for MR2 settings A6=0 and A7=0.
NOTE 4 Supplier data sheets include a max value for I_{DD6}.
NOTE 5 Applicable for MR2 settings A6=0 and A7=1. I_{DD6E} is only specified for devices which support the Extended Temperature Range feature.
NOTE 6 Refer to the supplier data sheet for the value specification method (e.g. max, typical) for I_{DD6E} and I_{DD6A}
NOTE 7 Applicable for MR2 settings A6=1 and A7=0. I_{DD6A} is only specified for devices which support the Auto Self Refresh feature.
NOTE 8 The number of discrete temperature ranges supported and the associated Ta - Tz values are supplier/design specific. Temperature ranges are specified for all supported values of T_{OPER}. Refer to supplier data sheet for more information.
NOTE 9 Applicable for MR2 settings MR2 [A7:A6 = 01] : Reduced Temperature range. IDD6R is verified by design and characterization, and may not be subject to production test

11.3 Electrostatic Discharge Sensitivity Characteristics - Q3'17 Ballot #1848.11

Table 129 — Electrostatic Discharge Sensitivity Characteristics

PARAMETER [1]	SYMBOL	MIN	MAX	UNIT	NOTES
Human body model (HBM)	ESD_{HBM}	1000	-	V	2
Charged-device model (CDM)	ESD_{CDM}	250	-	V	3

NOTE 1 State-of-the-art basic ESD control measures have to be in place when handling devices

NOTE 2 Refer to ESDA / JEDEC Joint Standard JS-001-2012 for measurement procedures.

NOTE 3 Refer to JESD22-C101F for measurement procedures

12 Electrical Characteristics & AC Timing

12.1 Reference Load for AC Timing and Output Slew Rate - No Ballot

DDR4 info as reference only

Figure 98 represents the effective reference load of 50 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

Ron nominal of DQ, DQS_t and DQS_c drivers uses 34 ohms to specify the relevant AC timing parameter values of the device.

The maximum DC High level of Output signal = 1.0 * VDDQ,

The minimum DC Low level of Output signal = { 34 /(34 + 50) } *VDDQ = 0.4* VDDQ

The nominal reference level of an Output signal can be approximated by the following:

The center of maximum DC High and minimum DC Low = { (1 + 0.4) / 2 } * VDDQ = 0.7 * VDDQ

The actual reference level of Output signal might vary with driver Ron and reference load tolerances. Thus, the actual reference level or midpoint of an output signal is at the widest part of the output signal's eye. Prior to measuring AC parameters, the reference level of the verification tool should be set to an appropriate level.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

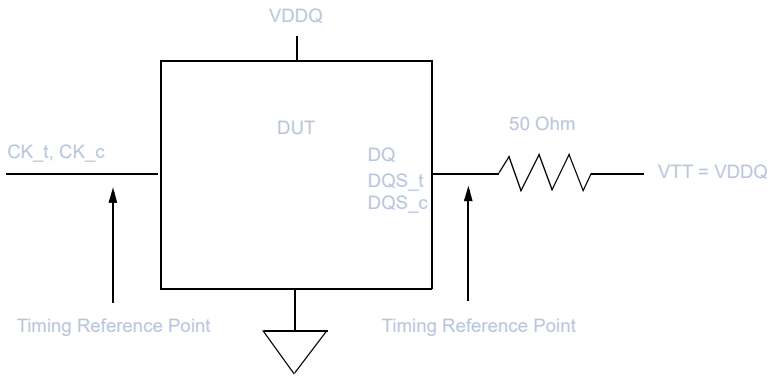


Figure 98 — Reference Load for AC Timing and Output Slew Rate

12.2 Timing Parameters by Speed Grade

12.2.1 Timing Parameters for DDR-3200 to DDR5-4000 - Q4'16 Ballot 1830.44A

Table 130 — for DDR5-3200 to DDR5-4000

Speed		DDR5-3200		DDR5-3600		DDR5-4000		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing									
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	8	20	8	20	ns	
Command and Address Timing									
CAS_n to CAS_n command delay for same bank group	tCCD_L	Max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	nCK	
WRITE CAS_n to WRITE CAS_n command delay for same bank group	tCCD_L_WR	Max(32nCK, 20ns)	-	Max(32nCK, 20ns)	-	Max(32nCK, 20ns)	-	nCK	
CAS_n to CAS_n command delay for different bank group for BL16, BC8(fixed) and BC8(on-the-fly)	tCCD_S	8	-	8	-	8	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	8	-	8	-	8	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 1KB page size	tRRD_S(1K)	8	-	8	-	8	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	8	-	8	-	8	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	Max(8nCK, 5ns)	-	nCK	
Four activate window for 2KB page size	tFAW_2K	Max(40nCK, 25ns)	-	Max(40nCK, 22.22ns)	-	Max(40nCK, 20ns)	-	nCK	
Four activate window for 1KB page size	tFAW_1K	Max(32nCK, 20ns)	-	Max(32nCK, 17.77ns)	-	Max(32nCK, 16ns)	-	nCK	
Four activate window for 1/2KB page size	tFAW_1/2K	Max(32nCK, 20ns)	-	Max(32nCK, 17.77ns)	-	Max(32nCK, 16ns)	-	nCK	
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	2.5	-	2.5	-	2.5	-	ns	
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	7.5	-	7.5	-	7.5	-	ns	
Internal READ Command to PRECHARGE Command delay	tRTP	7.5	-	7.5	-	7.5	-	ns	
WRITE recovery time	tWR	45	-	45	-	45	-	ns	

13 APPENDIX - Clock, DQS and DQ Validation Methodology - No Ballot

THIS AREA IS SUBJECT TO CHANGE BASED ON SUPPLIER & JEDEC FEEDBACK

13.1 Overview - No Ballot

This chapter describes the methodologies for validating specifications described in this document. Note that some of the methodologies in this document may reference qualitative means (for example, “slowly”, “a lot”). In such cases this document attempts to give some guidance as to what quantitative term should be assigned to those qualitative statements. However, it must be noted that the numbers assigned are not absolute.

13.2 Validation Equipment - No Ballot

Most of the voltage and timing measurements are performed using real time scopes and/or Bit Error Rate (BER) testers.

13.2.1 Oscilloscope

13.2.2 Bit Error Rate Tester (BERT)

13.3 DDR5 DRAM Input Clock Jitter Validation

13.3.1 Validation of DRAM Input Clock Jitter Specifications